Subject Date 1/3/2021 No.

+four modes of operation of transistor:

1- saturation: transistor functions as a short circuit between collector and emitter. $\beta I_B > I_C$

2- cut-off: transistor acts like an open circuit with no current flowing from collector to emitter.

3- forward active: the current from collector to emitter is proportional to the base current

4- reverse active: current flow of the forward active mode is reversed.

*"RTL": resistor-transistor logic *"DTL": diode-transistor logic

*"TTL": transistor-transistor logic *"ECL": emitter coupled logic

- designers should minimize the undefined input region while maximizing the noise margins as the output will be seen as either low (0) or high (1).

* RTL logic: 2/3/2021

assume the transistor is operating in one of the four modes until proven otherwise.

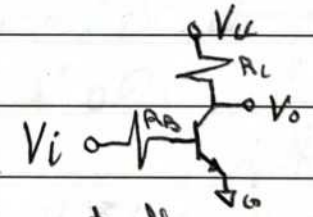
- forward-active: $V_{BE_{on}} = 0.7V$

- cut-off: $V_{BE} < 0.7V$

- saturation: $V_{BE_{sat}} = 0.8V$ ∧ $V_{CE_{sat}} = 0.2V$

- simple RTL inverter:

if $R_B = 10k$, $R_C = 1k$, $\beta = 50$, $V_{cc} = 5V$



∴ $V_o = V_{cc} - I_C R_C$

→ $I_C = 0$ → $V_o = V_{cc}$ ∧ $I_C = 0$ in cut-off

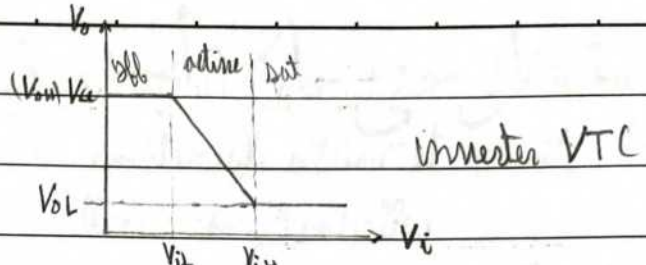
∴ $V_i \leq 0.7V$ → $V_o = V_{cc}$ → V_i = low → V_o = high

∴ $V_o = 0.2V$ in saturation → $I_C = \frac{V_{cc} - 0.2V}{R_C} = 4.8mA$

∴ $I_C = \beta I_B$ → $I_B = 96\mu A$ ∧ $-V_i + I_B R_B + V_{BE_{sat}} = 0$

→ $V_i = 0.8 + 96u \cdot 10k = 1.76V$ ∴ V_i = high → V_o = low

- "VTC": Voltage transfer characteristics



inverter VTC

- V_{iL}: maximum input voltage that will be recognized as low input logic level
- V_{iH}: the minimum input voltage that will be recognized as high input logic level
- V_{OH}: the output voltage recognized as logic high (corresponding to V_{iL} in inverter)
- V_{OL}: the output voltage recognized as logic level (corresponding to V_{iH} in inverter)

* noise margins: safety margins preventing erroneous outputs from noisy inputs
- if the output of one inverter is used as the input to the next:

→ $NM_L = V_{IL} - V_{OL} = 0.7 - 0.2 = 0.5V$

→ $NM_H = V_{OH} - V_{IH} = 5 - 1.96 = 3.24V$

where NM represents the noise margin and the subscript represents the logic level

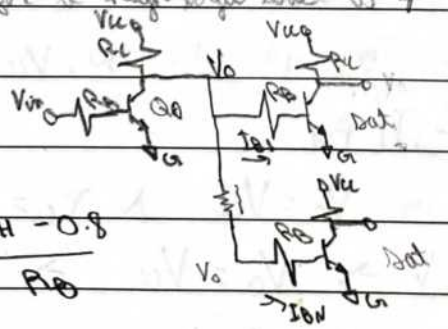
* fan-out: number of gate inputs driven by output of a single logic gate
- the maximum fan-out of an output measures its load driving capability
- the driving device must be able to supply (or sink) the sum of currents needed (or provided) by all the connected inputs while maintaining the output voltage specifications (to supply or sink depends on whether the output is a logic high or low level).

- for an RTL inverter, the fan-out for a low logic level is ∞.
- for an RTL inverter, the fan-out for a high logic level is $\neq \infty$

Ex1: if V_i = low → Q_0 off

→ V_o = high

∴ $V_o > V_{IH} = 1.96\,V$



$R_B = 10k\Omega$

$R_C = 1k\Omega$

$V_{BE\,Sat} = 0.8V$

$\therefore I_{C0} = N \cdot I_{B(1\to N)}$, $I_B = \frac{V_{iH} - 0.8}{R_B}$

$\therefore I_{C0} = \frac{V_{CC} - V_{iH}}{R_C}$

$\therefore \frac{V_{CC} - V_{iH}}{R_C} = N \cdot \frac{V_{iH} - 0.8}{R_B}$ → $N_H = \frac{R_B}{R_C} \cdot \frac{V_{CC} - V_{iH}}{V_{iH} - 0.8} = 33.75 \approx 33$

- $\beta I_B > I_C$ in saturation → $\sigma \cdot \beta \cdot I_B = I_C$ where σ: saturation parameter.
- in Ex 1, assume transistors are at end of saturation (EOS) → $\sigma = 1$

$\therefore I_{B(sat)} = \frac{I_{C(sat)}}{\beta} = \frac{V_{CC} - V_{CE(sat)}}{\beta \cdot R_C}$ ∧ $\beta = 50$

→ $I_{B(sat)} = 9.6 \times 10^{-5}$ A ∧ $I_{CO} = N \cdot I_{B(sat)} = \frac{5 - V_{IH}}{1k}$

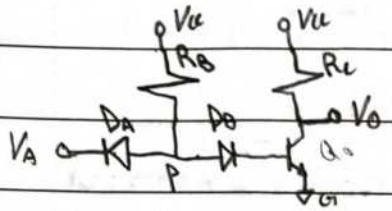
$\therefore N = \frac{3.24 \times 10^{-3}}{9.6 \times 10^{-5}} = 33.75 \approx 33$

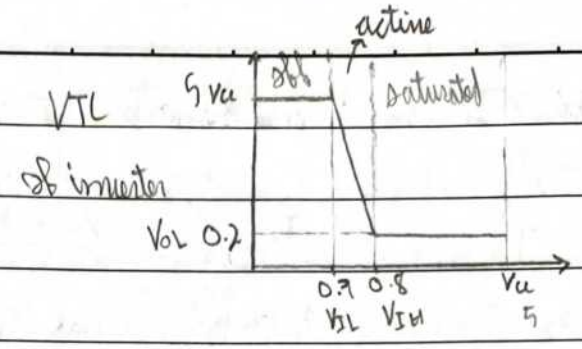
* fan-in: maximum number of inputs that a gate can have and maintain proper functionality
- for an RTL NAND gate, the fan-in is limited by the output voltage for low logic needs to be lower than V_{IL} (0.7)

Thus if $V_{CE(sat)} = 0.2$, max fan-in = $\frac{0.7}{0.2} = 3.5 \approx 3$ gates
- RTL was disadvantageous because transistors were the most expensive component (before IC technology), hence RTL was the dearest type of logic
- RTL dissipates high amounts of current, which causes a lot of losses to heat, hence RTL is not efficient.

Subject DTL (diode transistor logic) Date 12/3/2021 No.

* basic DTL inverter





assuming D_A is always on:

when $V_A = 0V$, $V_P = 0.7V$, $\therefore V_{BE(on)} = 0.7V \rightarrow Q_0$ is off

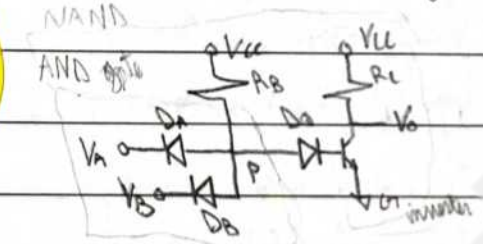
when $V_A = 0.7V$, $V_P = 1.4V \rightarrow Q_0$ is on (in active)

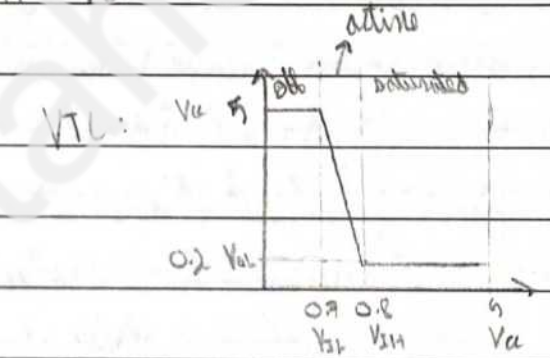
when $V_A = 0.8V$, $V_P = 1.5V \rightarrow V_{BE} = 0.8V \rightarrow Q_0$ is in saturation

$\therefore Q_0$ off for $0 \le V_A < 0.7$, active for $0.7 \le V_A \le 0.8$

& saturated for $0.8 < V_A \le V_{cc}$

* basic DTL NAND gate:





if V_A is grounded and D_A is assumed on:

$V_B = 0.5V$, $V_P = 0.7V$ (const) $\rightarrow D_B$ is off and $V_o = H$

$V_B = 1V$, $V_P = 0.7$ (const) $\rightarrow V_o = V_{cc}$ if $V_A = 0$ always

if V_B is grounded and D_B is assumed on:

$V_A = 0.7$, $V_P = 0.7V$, D_A is off, $V_o = H = V_{cc}$

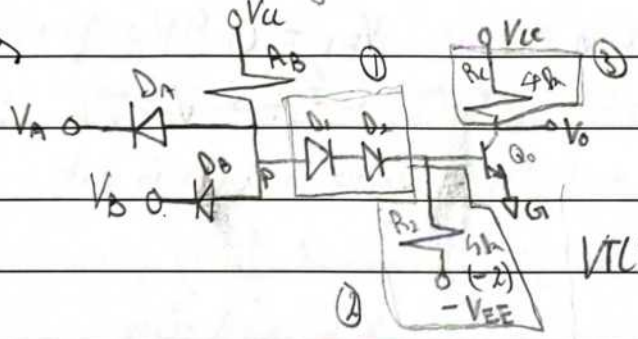
if V_B is fixed at 0.7V, $V_P = V_A + 0.7$ if D_A is on

$\rightarrow V_B = V_A = 0.7V \rightarrow V_P = 1.4V \rightarrow Q$ is in active

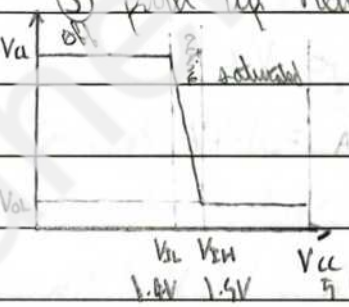
if $V_B = V_A = 0.8V \rightarrow V_P = 1.5V \rightarrow Q$ is in saturation

if V_B & $V_A > 0.8$, $V_o = 0.2V = L$

- level-shifting diodes are used to increase the noise margins by shifting V_{IL}.
- pull-up networks provide low resistance paths to V_{cc} when the transistor is off and high resistance paths when transistor is saturated.
- pull-down networks provide a path for collected charge when the transistor goes from saturation mode to cut-off.



① level-shifting diodes
② pull-down network
③ pull-up network



- $-V_{EE}$ in the pull down network (can be 0V (but it is given a negative to speed up the discharging)
- (Reminder): if the transistor is in saturation mode, charges accumulate in the base terminal (can be represented by a capacitor connecting the base and emitter). Hence, to turn off a transistor, the charges accumulated at the base must be removed.
- the fan-out for the high output of a DTL NAND gate is considered ∞ since no current flows through the input diodes. $\therefore N_H \to \infty$

opposite to RTL

$\therefore$ Q_0 must remain saturated $5 V_A$ $5 V_B$

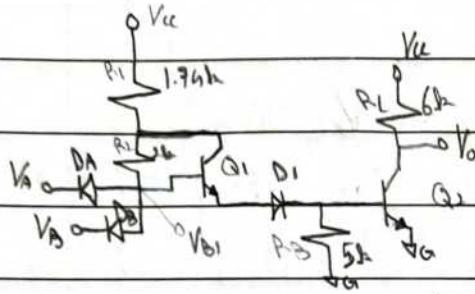
$\to I_{C0(sat)} \leq \beta I_B$

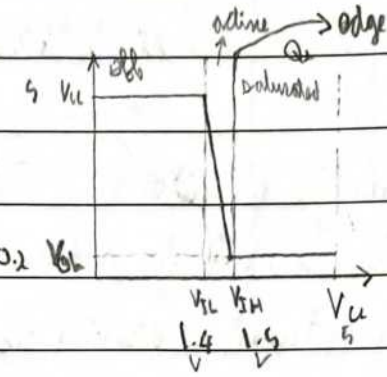
$\wedge I_{C0(sat)} = N \cdot I_{DA} + \frac{5}{4k}$

$\to N \cdot I_{DA} = \beta I_B \quad \wedge I_B = 0.84\ mA \quad \wedge I_{DA} = 1.75\ mA \to N = \frac{50 \cdot 0.84\ mA - 1.25\ mA}{1.75\ mA} = 23.28 \approx 23$

- smaller σ indicates transistor is more saturated

* modified DTL NAND:





If V_B is fixed at 5V ($=V_{cc}$):

- If $V_A = 0.2V$ (low) and D_A is on → $V_{B1} = 0.9V$ → Q_1 is sat, but D_1 is off → Q_1 is off and Q_2 is off → $V_o = V_{cc}$
- If $V_A = 5V$ → Q_1 is sat and D_1 is active and Q_2 is sat → $V_o = V_{cc}$
- When $V_A = 1.4V$ ∧ D_A is on → Q_1 is forward active ∧ Q_2 is forward active
- When $V_A = 1.5V$ ∧ D_A is on → Q_1 is sat ∧ Q_2 is sat → $V_o = V_{cc}$

∴ $V_{IL} = -D_{A(on)} + V_{BE1(on)} + D_{1(on)} + V_{BE2(on)} = 1.4V$

∧ $V_{IH} = -D_{A(on)} + V_{BE1(on)} + D_{1(on)} + V_{BE(sat)} = 1.5V$

If $V_A = 0.2V$ → Q_1 ∧ Q_2 are off, assuming D_A is on

→ $V_{B1} = 0.4V$ ∴ $I_A = \frac{V_{cc} - 0.9}{3.74k} = 1.093\,mA$ (all other currents = 0)

If $V_A = V_B = V_{cc}$ ∧ D_1 is on, Q_1 is forward active ∧ $\beta = 100$

→ $V_{B1} = V_{BE1(on)} + V_{D1(on)} + V_{BE2(sat)} = 2.2V$

∵ $I_{A1} = I_{B1} + I_{C1} = I_{E1}$ → $I_{B1} = \frac{I_{R1}}{\beta+1}$

→ $-5 + I_{R1} \cdot 1.94k + I_{B1} \cdot \frac{2k}{\beta+1} + 2.2 = 0$ → $I_{A1} = \frac{2.8}{1.94k + \frac{2k}{101}}$

→ $I_{R1} = 1.582\,mA$

∵ $V_{BE2} = 0.8V$ ∧ $I_{E1} = I_{B2} + I_{RB2}$

→ $I_{B2} = 1.582\,mA - \frac{0.8}{5k} = 1.422\,mA$

∧ $I_{L2} = \frac{5-0.2}{6k} = 0.8\,mA$

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- for a high output from a modified DTL NAND, an ∞ number of gates can be driven

- for a low output, the transistor Q_1 must remain saturated

$\rightarrow \beta I_{B1} \geq I_{C1}$, $I_{C1} = N \cdot I_{BN} + I_{R1}$

$\therefore I_{BN} = \frac{V_{cc} - 0.9}{3.9k\Omega} \approx 1.093mA$

$\therefore \beta I_{B1} = 100 \cdot 1.422mA = 142.2mA$ (or 91.1mA)

$\therefore N \cdot I_{BN} + \frac{5 - 0.2}{6k} \geq \beta I_{B1} \rightarrow (\beta = 100)\ N = 129$

$(\beta = 50)\ N = 64$

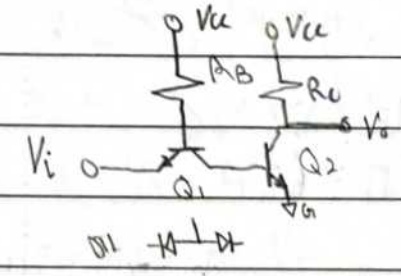
- the average power dissipation is given by:

$$P(avg) = V_{cc} \cdot \frac{I_{cc}(@H) + I_{cc}(@L)}{2}$$

Subject TTL (transistor-transistor logic) Date 14/3/2021 No.

- in designing ICs, compactness and logic density are most important. Since resistors and capacitors are generally the largest components, reducing their count will free up space for extra transistors and save costs
- TTL logic still requires resistors, whereas MOS gates can be made of transistors only. Hence why they are more ubiquitous today.

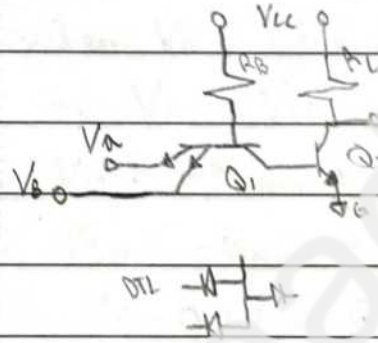
+ Basic TTL inverter:



DTL

When V_i is high, Q_1 is on, pushing Q_2 into saturation → V_o = L (0.2V)
When V_i is low, the accumulated charges at the base terminal of Q_2 will have a path to the emitter of Q_1, hence turning Q_2 off.

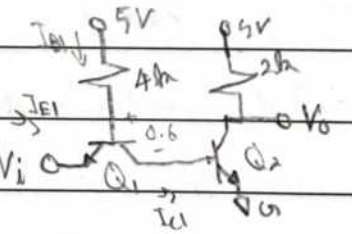
+ Basic TTL NAND gate:



DTL

Q_1 is a multi-emitter bjt
D_1: Composite (Darlington pair) diode

+ for a basic TTL inverter:



if V_i = 0.2, assuming Q_1 is in sat:
→ V_{B1} = 0.2 + 0.8 = 1V ∵ $V_{BE(sat)}$ = 0.8V
→ I_{B1} = 1mA = I_{E1}
∧ I_{B2} = 0 → Q_2 is off → V_o = V_{cc} = 5
if V_i = 5V, assuming Q_2 is in sat ∧ Q_1 is in reverse active
∴ $V_{BC(on)}$ = 0.6V ∧ $V_{BE(sat)}$ = 0.8V → V_{B1} = 1.4V
∴ I_{C1} = I_{B2} = $(\beta_{N}+1)\cdot I_{B1}$ where β_N is the reverse beta = 0.1

∴ $I_{B1} = \frac{5-1.4V}{4k} = 0.9mA \rightarrow I_{C1} = (1+0.1)\cdot 0.9mA = 0.99mA$

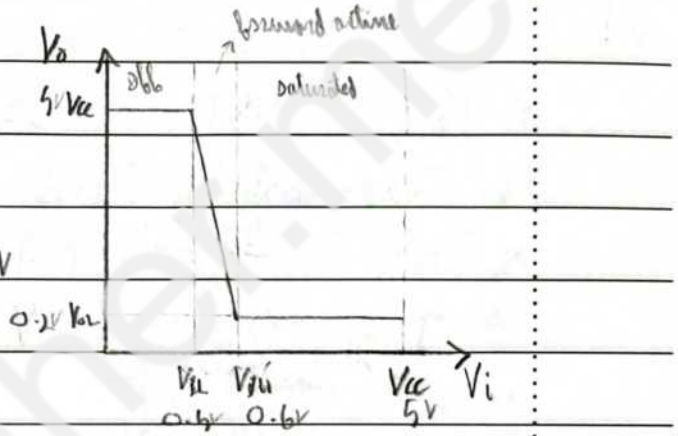
∴ $I_{E1} = B_{R1} \cdot I_{B1} = 0.09mA$

∵ $I_{C2} = \frac{V_{cc} - V_{CE(sat)}}{2k} \rightarrow I_{C2} = \frac{5-0.2}{2k} = 2.4mA$

∵ for saturation, $I_C < BI_B$ ∴ $B_2 = 50$

∴ $I_{C1} = 2.4mA < 50 \cdot 0.99mA = B_2 I_{B2}$ ∴ Q_2 is saturated.

+ VTC for basic TTL inverter: Q_2:



if $V_i = 0.2V$, off.

Q_2 can turn on when $V_{BE2} = 0.9V$

$\rightarrow V_{B1} = 0.6 + 0.9 = 1.3V \rightarrow V_i = 0.6V$

∵ $V_{BC(on)} = 0.6V$

- the voltage for $V_{BC(on)}$ is less than $V_{BE(on)}$ because transistors are not symmetrical and the emitter is more heavily doped compared to the collector.
- immediately after switching an input of a basic TTL inverter from high (5V) to low (0.2V):

Q_1 turns to forward active $\rightarrow V_{B1} = V_i + V_{BE(on)} = 0.4V$

momentarily, Q_2 will remain saturated $\rightarrow V_{B2} = 0.8V = V_{BE(sat)}$ (due to propagation delay)

Q_2 immediately changes to forward active since $V_{B2} = 0.8V$

∴ $V_i = 0.2V \rightarrow V_{CE1} = 0.6V > V_{CE1(sat)} = 0.2V$

therefore, a voltage larger than the saturation voltage keeps the transistor unsaturated.

∵ $I_{B1} = \frac{5-0.9}{4k} = 1.025mA$

$\rightarrow$ initial $I_{C1} (= I_{B2}) = BI_{B1} = 51.25mA$

fan-out for TTL inverter:

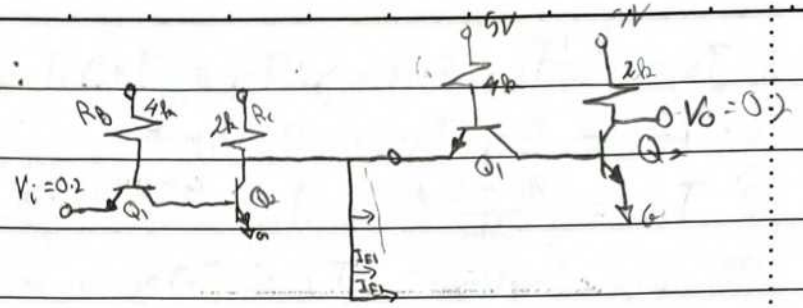
- low input case:

∵ Q_1 is sat (stage 1)

Q_2 should be off

→ Q_1 of next stage should be reverse active

→ Q_2 should be sat



→ $V_{BE22} = 0.8V$ ∧ $I_{B22} = I_{E12} + I_{B12}$ ∧ $I_{E1} = \beta_1 I_{B1}$

for Q_{22} sat, Q_{12} reverse active → $V_{B12} = 0.6 + 0.8 = 1.4V$

→ $I_{B12} = \frac{5-1.4}{4k} = 0.9mA$ → $I_{E12} = \beta \cdot 0.9mA$

∵ $I_{C21} = \frac{5-V_o}{2k} = N \cdot \beta_{R1} \cdot (0.9)$, $\beta_{R1} = 0.1$ ∧ $V_o = H \Rightarrow V_o \geq 4.2V$

↳ Reverse beta

∴ $I_{C21} = \frac{5-4.2}{2k} = N \cdot 0.1 \cdot 0.9m = 4.444 \Rightarrow \boxed{N_{max} = 4}$

- high-input case: $V_i = 5$

→ Q_{11} is reverse active, Q_{21} is sat, Q_{12} is sat, Q_{22} is off

→ $V_{B21} = 0.8V$ → $V_{B11} = 0.8 + V_{BC(reverse\ BJT)} = 1.4V$

∵ for Q_{21} to remain in sat: $\beta \cdot I_{B21} \geq I_{C21}$

$I_{C21} = I_{BC21} + N \cdot I_{E12}$ ∧ $I_{E12} = I_{B12} = \frac{5-(0.2+0.8)}{4k}$

↓ $I_{BC21} = \frac{5-0.2}{2k} = 2.4mA$

∧ $I_{B21} = I_{C11} = I_{B11} + I_{E11}$, $I_{B11} = \frac{5-1.4}{4k} = 0.9mA$

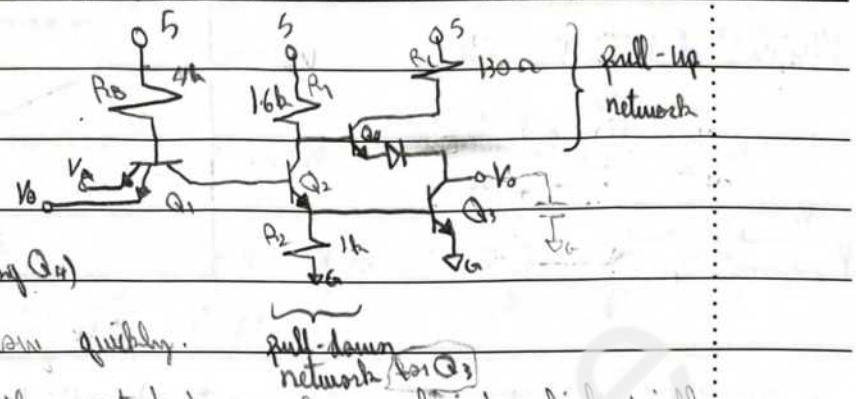
↓ $I_{E11} = \beta_{R1} \cdot 0.9mA = 0.09mA \Rightarrow I_{C11} = 0.99mA$

∴ $(0.99mA) \cdot \beta \geq 2.4mA + N \cdot (1mA)$

→ $N = \frac{0.99mA \cdot \beta - 2.4mA}{1mA}$ ∧ $\beta = 50 \Rightarrow \boxed{N = 47}$

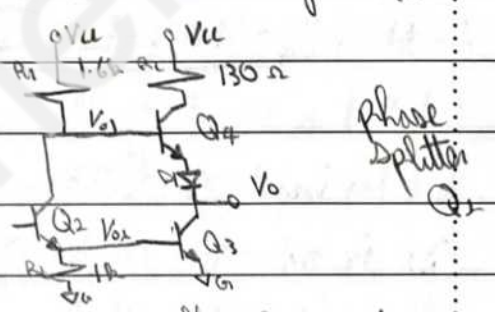
Subject Date No.

* Standard TTL NAND gate:



- Q_4 is included as a consequence to including Q_4.
- since the pull-up network (including Q_4) allows V_o to go from high to low quickly.
- The pull-down network allows the output to go from low to high quickly
- Transistor Q_2 is included to control Q_4. When output is low, Q_3 is saturated by the input current from Q_2, which is also saturated causing the base voltage of Q_4 to be 0.2V and cutting it off.
- Q_2 is called a phase splitter:

* Phase splitter: allows the input condition to be produced in opposite phases; allowing Q_3 to be on while Q_4 is off



if V_i = low, $V_{o1} = V_{cc}$ & $V_{o2} = 0$ → Q_3 = off, Q_4 = sat

if V_i = high, $V_{o1} = 0.9$V & $V_{o2} = V_{BE3}$ → Q_3 = on, Q_4 = off

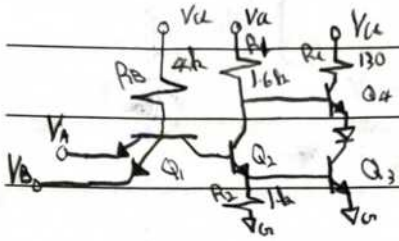
Diode D_1 is included to keep transistor Q_4 off even when $V_{o1} = 0.9$V

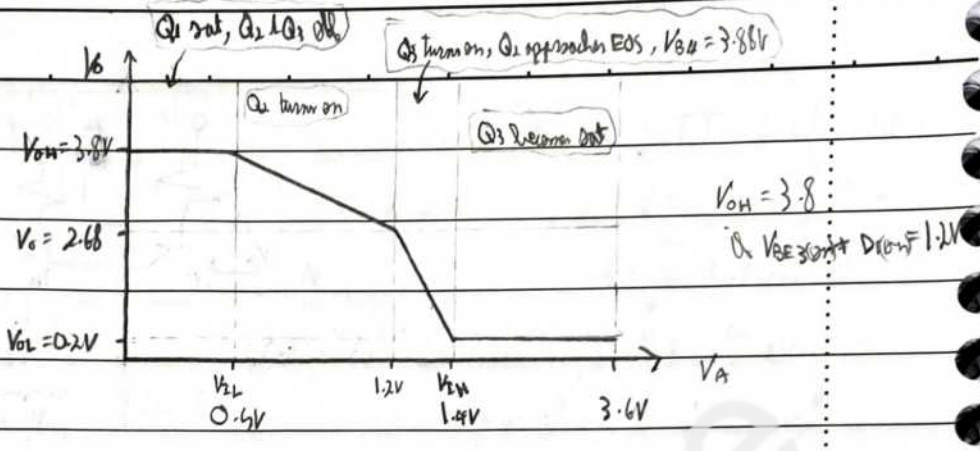
hence, 0.9V at base terminal of Q_4 can be considered low

- output transistor pair, Q_3 & Q_4, along with diode, D_1, are referred to as the totem pole output
- totem pole output configuration can actively source or sink current and is useful for capacitive loads.
- diode, D_1, increases the effective turn-on voltage of Q_4, allowing Q_4 to be turned off before Q_3 is fully on, preventing large surge currents from flowing in the output stage during transitions from high to low or vice versa
- the diode causes the output high voltage level to be reduced by the voltage drop across the diode

Subject Date No.

VTL of standard TTL NAND gate:





- When V_A & V_B are low, Q_1 is saturated, the base current of Q_1 goes to the emitters, Q_2 gets no base current and is off causing Q_3 to be off as well. V_o is high (there is an added voltage drop due to diode D_1), (Q_4 in Act)
- If either input (or both) are increased then some of the base current is directed to the collector of Q_1, base of Q_2 and causes it to turn on (active mode) and sinks a current to the base of Q_3, turning it on in turn.
- If either input (or both) are high, Q_1 is in reverse active mode, Q_2 is saturated, causing Q_3 to saturate as well. Hence Q_4 will be off and V_o will be low (0.2V)

$NM_H = 3.8 - 1.4 = 2.4V$

- Noise margins in the above circuit are unequal: $NM_L = 0.5 - 0.2 = 0.3V$

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① $V_{CC} = 5$, $\beta = 96.6$, $R_L = 2k$

$$\frac{2 - 0.8}{R_B} = \frac{5 - 0.2}{2k \cdot 96.6} = 483\,\Omega$$

② $\sigma \beta \cdot I_B = I_{cont}$ $I_{cont} = \frac{5 - 0.2}{4k} = 1.2\,mA$

$$I_B = \frac{-0.8}{5k} + \frac{5 - 2.2}{2.08k} = 1.1861\,mA$$

$$\Rightarrow \sigma = 0.0155$$

③ $\sigma = 0.9 \rightarrow 0.9 \cdot 50 \cdot I_B = \frac{5 - 0.2}{1k}$

$$\rightarrow I_B = \frac{4.8m}{0.9 \cdot 50} = 0.106667\,mA$$

$$\therefore V_i = 0.8 + I_B \cdot R_B = 2.197$$

④ $\frac{5 - V_o}{R_L} = \frac{V_o - 0.8}{12.8k}$

$$\Rightarrow 5 - V_o = \frac{6 \cdot 1k}{12.8k} \cdot (V_o - 0.8)$$

$$\Rightarrow 5 + \frac{6 \cdot 0.8}{12.8} = V_o \left(\frac{6}{12.8} + 1\right)$$

$$\rightarrow V_o = 3.659\,V$$

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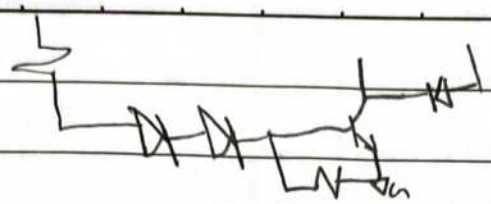
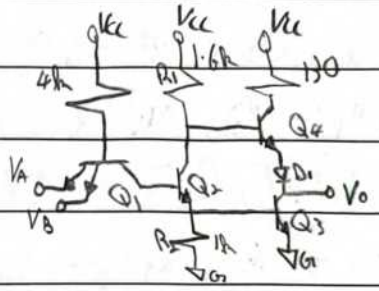
④



$I_C = \frac{5 - 0.2}{4\Omega} + \frac{5 - 0.7}{2.4\Omega} = 1.2 +$

* high output:



when either (or both) inputs is low, the output will be high

* EOC: edge of cutoff

$0 < V_A$ or $V_B < 0.5$

assume Q_1 is sat, $V_A = 0.2V \rightarrow V_{B1} = V_{BE(on)} + 0.2V = 1V$

$\rightarrow I_{B1} = \frac{5-1}{4k} = 1mA$ goes to A or B (emitter)

$\therefore$ Q_1 is sat $\rightarrow V_{CE} = 0.2V \rightarrow V_{B2} = 0.4V$

$\therefore$ $V_{B2} < V_{BE(on)} \rightarrow Q_2$ is off $D_1 \wedge Q_4$ is at EOC

$\therefore$ Q_2 is off $\rightarrow I_{B3} = 0 \rightarrow Q_3$ is off

$\therefore$ V_o is unconnected, no current flows through Q_4 or D_1

$\rightarrow V_o = V_{CC} - V_{BE4(on)} - D_{1(on)} = 5 - 0.7 - 0.7 = 3.6V$ (3.8V)

$I_{EB} = 0$ if V_B is high / $I_{EB} = I_{EA} = \frac{I_B}{2}$ if $V_A = V_B =$ low

* indeterminate: Q_2 is active (npn) when $0.5V < (V_A$ or $V_B) < 1.2V$

assuming Q_1 is sat $\rightarrow$ $1.3V < V_{B1} < 2V \rightarrow 0.7V < V_{B2} < 1.4V$

$\rightarrow$ $0V \leq V_{E2} < 0.7V = V_{B3} \rightarrow V_{B3}$ off

$\therefore$ V_o is open, $I_{E4} = 0$, $I_{B4} = 0$, $D_1 \wedge Q_4$ are at EOC

$\wedge$ $I_{C2} = I_{A1} = I_{E2}$ $\wedge$

$\rightarrow I_{E2} = \frac{V_{B2} - V_{BE(on)}}{R_2} \rightarrow 0 < I_{B1} < 0.7mA$

$\therefore V_o = V_{CC} - I_{B1} \cdot R_1 - V_{BE4(on)} - D_{1(on)}$

$= 5 - I_{B1} \cdot 1.6k - 0.6 - 0.6 \rightarrow \boxed{2.68V < V_o < 3.8V}$

$\therefore V_{B4} = V_{CC} - I_{B1} \cdot R_1 = 3.88V \wedge V_{CE} = V_{B4} - I_{E1} \cdot R_2$

$\wedge I_{E1} = I_{C1} = I_{B1}$ when $0.7 < V_{B2} < 1.4 \rightarrow V_{CE} = 3.18V$

$\therefore$ Q_2 is not in sat but in active forward.

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* indeterminate : Q_3 is active, Q_2 is active, Q_1 is sat

when $0.7V < V_{E2} < 0.9V$, Q_3 will be active

→ $1.4V < V_{B2} < 1.6V$ → $1.2V < (V_A \text{ or } V_B) < 1.4V$

∴ $V_B = V_{CC} - I_{B1} \cdot R_1 - V_{BE4(on)} - D_{1(on)}$

∴ $\boxed{V_B = 3.6 - I_{B1} \cdot R_1}$

∧ $I_{B1} = I_{C2} + I_{B4}$ ∧ $I_{E2} = I_{C2} = I_{B2} + I_{B3}$

∧ $I_{B2} = \frac{V_{BE2} - 0.7}{R_2}$

* low output : when both V_A & V_B are high → $(V_A \& V_B) > 1.4V$

→ Q_1 is in reverse active, $V_{BC(rev)} = 0.6V$

→ Q_2 & Q_3 are in sat → $V_{B2} = V_{BE2(sat)} + V_{BE3(sat)} = 1.6V$

→ $V_{B1} = 1.6 + V_{BC(rev)} = 2.2V$ → $I_{B1} = \frac{5-2.2}{4k} = 0.7mA$

→ $I_{C1} = (1 + B_{reverse}) \cdot I_{B1}$, assuming $B_{reverse} = 0.1$

→ $I_{C1} = 0.77mA = I_{B2}$

∴ Q_2 is sat → $V_{CE2} = V_{CE2sat} = 0.2V$

∧ $V_{E2} = 0.8V$ → $V_{C2} = V_{B4} = 1V$ ∴ Q_4 off (diode is off.)

∧ $I_{R1} = \frac{5-1}{R_1} = 2.5mA = I_{C2}$

∴ $I_{E2} = I_{C2} + I_{B2} = 2.5 + 0.77 = 3.27mA$

∧ $I_{E2} = I_{B3} + I_{B2}$ ∧ $I_{B2} = \frac{V_{E2} - 0}{R_{2a}} = 0.8mA$

→ $I_{B3} = 2.47mA$ ∧ $V_B = 0.2V$ (low)

∴ $\beta I_B > I_C$ for sat, $I_{C3} = 0$ → Saturated

- If D_1 is not used, when Q_1 is rev. active and Q_2 & Q_3 are sat

∴ $V_{B4} = 1V$ → Q_4 will be sat → $V_{C4} = V_{CE4sat} + V_{CE3sat}$

→ $I_{C4} = I_{RC} = \frac{V_{CC} - 0.4}{130} = 35.38mA$ → $P = 163mW$

hence, a lot of power is being dissipated for no reason and the large current can burn the circuit

* fan-out for low output logic:

$\therefore \quad \beta I_B > I_C \rightarrow \sigma \beta_3 I_{B3} = I_{C3}$

for $\sigma = 1$ $\beta_3 = 10$, $I_{B3} = 2.47\ mA$ (calculated previously)

$\rightarrow 24.7\ mA = I_{C3} \cdot N$

$\wedge\ I_{C3} = I_{AN}$ (or I_{BN}), assuming other input in next stage is high

$I_{AN} = I_{ABN} = \frac{V_{CC} - V_{BIN}}{R_{BN}}$, $V_{BIN} = V_\beta + V_{CE(sat)} = 1V$

$\rightarrow I_{AN} = 1mA$

$\therefore 24.7mA = N \cdot 1mA \rightarrow \boxed{N = 24}$

* fan-out for high output logic:

if $V_{O(min)} = 3.3V$ $\wedge\ \beta_4 = 100$

$\rightarrow I_{EC4} = (1+\beta) \cdot I_{B4} = N \cdot I_{EIN}$ $\wedge\ I_{EIN} = I_{CIN} - I_{BIN}$

$\wedge\ I_{BIN} = \frac{5 - V_{BIN}}{4k}$ $\wedge\ V_{BIN} = V_{BE(on)} + V_{BE(sat)} + V_{BE(sat)}$

$\rightarrow V_{BIN} = 2.1V \rightarrow I_{BIN} = \frac{2.8}{4k} = 0.7mA$

$\wedge\ I_{EIN} = I_{BIN} \cdot \beta_{FOR} = 0.1 \cdot 0.7mA = 0.07mA$

$\therefore 101 \cdot I_{B4} = N \cdot 0.07$

$\wedge\ I_{B4(max)}$: $V_{B4} = 3.3 + 0.7 + 0.7 = 4.7V$

$\rightarrow I_{B4(max)} = \frac{5 - 4.7}{1.6k} = 0.1875\ mA$

$\therefore (101) \cdot (0.1875\ mA) = N \cdot 0.07$

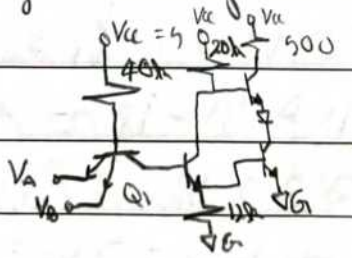
$\rightarrow N = 270$

* low-power TTL: achieved by increasing the resistances as shown

$P_H = \frac{5-1}{40k} \cdot 5 = 0.5mW$

$P_L = 0.07 \cdot 5 + 0.2 \cdot 5 = 1.35mW$

$\rightarrow P_{avg} = \frac{1.35 + 0.5}{2} = 0.925mW$



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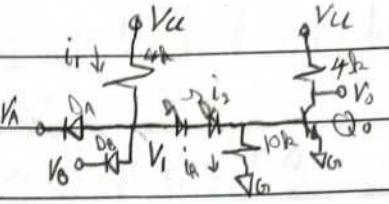
Example 17.8:



assuming logic 0 = 0.1V ∧ $V_A = V_B = 0.1V$

if D_A ∧ D_B active ⇒ $V_1 = 0.8V$

∴ D_1 ∧ D_2 off ∧ $i_1 = 1.05mA$, Q_0 is off ∧ $V_0 = V_{CC}$

if $V_A = V_B$ = logic 1 = 5V ⇒ D_A ∧ D_B off, D_1 ∧ D_2 on ∧ Q_0 sat

⇒ $V_1 = V_{BE(sat)} + V_{D1\,on} + V_{D2\,on} = 2.2V$

∧ $i_2 = i_1 = \frac{5-2.2}{4k} = 0.7mA$

Confirm sat: $\beta I_B > I_C$, $I_C = \frac{5-0.1}{4k} = 1.225mA$

∧ $I_B + I_R = I_2 = I_1$, $I_R = \frac{0.8}{10k} \Rightarrow I_B = 0.62mA$

∧ $\beta = 25 \Rightarrow \beta I_B = 15.5mA > 1.225mA$

Ex 17.8:

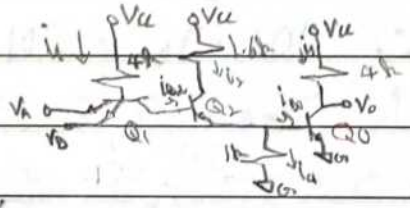
$P_H = V_{CC} \cdot i_{1H} + V_{CC} \cdot I_{CH} = 9.625mW$

$P_L = V_{CC} \cdot i_{1L} = 5.25mW$

P_L if $V_A = V_B = 0V \Rightarrow V_1 = 0.9V \Rightarrow i_1 = 1.075mA$

∴ $P_L = 5.375mW$

example 17.9:



if $V_A = V_B = 0.1V$ ∧ Q_1 is sat

⇒ $V_{B1} = 0.9V \Rightarrow i_2 = 1.025mA$

⇒ Q_2 is off ∧ Q_0 is off ⇒ $V_0 = V_{CC}$

if $V_A = V_B = 5V$, Q_1 is reverse active ∧ Q_2 is on ∧ Q_0 is sat

⇒ $V_{B2} = V_{BE0\,sat} + V_{BE2\,sat} = 1.5V \Rightarrow V_{B1} = 1.5 + V_{BC(reverse\,active)}$

∴ $V_{B1} = 2.3V \Rightarrow i_1 = \frac{2.3}{4k} = 0.675mA$

⇒ $I_{B2} = (1 + \beta_{rev}) \cdot i_1 = 0.742.5mA$

∵ Q_2 is sat ∧ $V_{B0} = 0.8V \Rightarrow V_{C2} = 1V \Rightarrow i_2 = \frac{4}{1.6k}$

∴ $i_{E2} = i_2 + i_{B2} = 3.242.5mA = i_4 + i_{B0}$ ∧ $i_4 = \frac{0.8}{1k}$

⇒ $i_{B0} = 2.442.5$

Confirm sat: $\beta \cdot i_{B0} > i_{C0}$

$25 \cdot 2.442.5 > \frac{4.8}{4k}$

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Ex 17.9:

a) ∵ $V_x = V_y = 0.1V$, Q_1 is sat, $i_1 = \frac{5-0.9}{12k} = 0.34167\ mA$

Q_2 & Q_3 are cutoff → $i_2 = i_3 = i_{E2} = 0$ ∧ $V_o = V_{cc}$

b) $V_x = V_y = 5V$, Q_1 is Reverse active, Q_2 ∧ Q_3 are sat

→ $V_{B1} = 2.3V$ → $i_1 = \frac{2.7}{12k} = 0.225\ mA$ → $i_{B2} = 0.2475\ mA$

∵ Q_2 is sat → $V_{C2} = 0.8 + 0.1$ → $i_2 = \frac{4.1}{4k} = 1.025\ mA$

∴ $i_{E2} = i_{B2} + i_2 = 1.2725\ mA = i_{B3} + i_4$ ∧ $i_4 = \frac{0.8}{2k}$

→ $i_{B3} = 0.8725\ mA$ ∧ $i_3 = \frac{4.9}{6k} = 0.8167\ mA$

confirm sat: ∵ $i_B > i_C$ → $25 \cdot 0.8725 > 0.8167$

example 17.10:

∵ ∵ $I_B > I_C$ → $25 \cdot 2.4425 = N \cdot i_1 + 1.025$

∧ $i_1 = 1.025\ mA$ → $N = 58$

Ex 17.10:

When $V_x = V_y = 3.6V$ → Q_1 is Rev active, Q_2 ∧ Q_3 are sat

→ $V_{B1} = 2.3V$ → $i_{B1} = 0.225\ mA$ → $I_{C1} = 0.27\ mA$

∵ Q_2 is sat → $V_{B2} = 0.9V$ → Q_3 is cutoff ∧ $i_{C2} = 1.025\ mA$

→ $i_{E2} = 1.025 + 0.27 = 1.295\ mA = i_{ABO} + i_{BO}$

→ $i_{BO} = 0.895$ → $V_o = 0.1$

to keep sat: $25 \cdot 0.895 = N \cdot \frac{5-0.9}{12k}$ → $N = 65$

to keep $I_C = 12mA$ → $12mA = N \cdot \frac{5-0.9}{12k}$ → $N = 35$

TYU 17.5:

a) $i_1 = \frac{4.2}{15k} = 0.28\ mA$, $i_2 = 0 = i_A = i_{AL} = (b)$

c) $i_1 = i_2$, Q_3 is sat → $V_B = 0.8$ → $V_1 = 2.2V$ ∧ $i_F = 0.18667\ mA$

$i_B = i_2 - i_A = 1.33 \times 10^{-4}\ A$ ∧ $i_R = 0.05333\ mA$

$i_{AL} = \frac{5-0.1}{6k} = 0.817\ mA$ ∧ $V_o = 0.1V$

TYU 17.6:

for low output: $i_B = 0.1333\ mA$ ∧ $i_L = 0.8167\ mA$

a) $\beta \cdot i_B > i_L$ for sat

→ $\beta \cdot i_B = i_L + N \cdot \frac{4.2}{150}$ → $N = 11$ ×(N=9 in book)

b) $I_{C,max} = 12mA = i_{BL} + N \cdot \frac{4.2}{150}$ → $N = 39$ ×(N=9 in book)

TYU 17.7:

low output: $i_B = 0.8167\ mA$ ∧ $i_{BO} = 0.895$

→ $25 \cdot 0.895 = 0.8167 + N \cdot 0.3482$ → $N = 63$

17.19:

a) i) if $V_i = 0.1\ V$ → D_1 is active, Q_0 in cut off → $i_1 = 0.141667\ mA$

$i_2 = i_3 = 0$ ∧ $V_1 = 0.8V$ ∧ $V_2 = V_{CC} = 2.5V$

ii) if $V_i = 2.5\ V$ → D_1 is off, Q_0 in sat → $V_1 = 1.5\ V$

∧ $i_2 = i_1 = \frac{1}{12k} = 0.0833\ mA$, $V_0 = 0.4V$ → $i_3 = 0.2\ mA$

∵ $\beta \cdot i_2 > i_3$ → $25 \cdot 0.0833 > 0.2$ → sat

b) at Q_0 EOL → $V_1 = 1.4V$ → $V_I = 0.9V$

at Q_0 EOS → $V_1 = 1.5$ → $V_I = 0.8V$

17.20:

a) if $V_I = 0V$ → $V_1 = 0.7V$, $i_1 = 0.4333\ mA$, $i_B = 0 = i_C$

∧ $V_0 = 3.3V$

b) if $V_I = 3.3V$ → $V_1 = 1.5V$ → $i_1 = 0.3\ mA$

$i_B = i_1 - \frac{0.8}{20k} = 0.26\ mA$, $V_0 = 0.1V$ ∧ $i_C = 0.8\ mA$

confirm sat: $0.26 \cdot \beta = 6.5\ mA > 0.8\ mA$ ✓

17.21:

i) if $V_x = V_y = 0.1$ → $V = 0.8V$ → $i_1 = 0.525\ mA$

$i_3 = i_2 = 0\ A$ ∧ $V_0 = 5V$

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ii) $V_x = V_y = 5V \Rightarrow V' = 2.2V$, $i_1 = 0.365mA = i_4 + \frac{0.8}{15k} \Rightarrow i_4 = 0.2967mA$

$\wedge\ i_3 = \frac{4.9}{2.4k} = 2.042\ mA$

17.22:

i) $i_1 = 0.3125mA \wedge V' = 0.8V$, $i_4 = i_3 = 0 \wedge V_o = 3.3V$

ii) $i_1 = 0.1395mA \wedge V' = 2.2V$, $i_4 = i_1 - \frac{0.8}{15k} = 84.167\mu A$

$\wedge\ i_3 = 1.33\ mA$

17.23:

a) $Q_1 \wedge Q_2$ sat $\Rightarrow V_1 = 2.3V \Rightarrow i_1 = 0.695mA = i_{B1}$

$\wedge\ i_2 = \frac{3.4}{2k} = 1.7\ mA \quad \therefore i_4 = 2.395mA$

$i_{B2} = i_4 - i_5 = 2.195\ mA \quad \wedge\ i_3 = \frac{4.9}{4k} = 1.225mA$

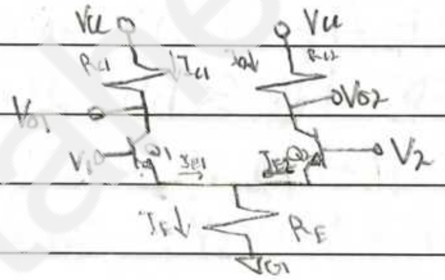
b) $\because \beta \cdot i_{B2} = 1.225 + N \cdot \frac{4.2}{4k}$

$\Rightarrow N = 42$

Subject: emitter coupled logic Date: 6/4/2021 No.

- main ECL advantage is the very short propagation delay.
+ disadvantages include:
  - high power consumption
  - poor speed-power product
  - low level of integration
  - not compatible with TTL and CMOS
- ECL logic and interface technology is still used in very high-speed communications gear such as fiber optic transceiver interfaces and asynchronous transfer mode networks (ATM)

* basic ECL current switch:



if $V_1 < V_2$

Q_1 is off, V_{o1} is high

Q_2 is forward active, V_{o2} is low

if $V_1 > V_2$

Q_2 is off, V_{o2} is high

Q_1 is FA, V_{o1} is low

hence, V_{o1} is the inverting output while V_{o2} is the non-inverting if V_2 is fixed.

assuming Q_1 and Q_2 are forward active:

$\rightarrow V_{o1} = V_{CC} - I_{C1} \cdot R_{C1}$ ∧ $V_{o2} = V_{CC} - I_{C2} \cdot R_{C2}$

∧ $I_E = I_{E1} + I_{E2}$, ∵ $\alpha = \frac{\beta}{\beta + 1}$, $\alpha_1 = \alpha_2 = \alpha$

$\rightarrow I_E = (I_{C1}/\alpha_1) + (I_{C2}/\alpha_2) \rightarrow \alpha I_E = I_{C1} + I_{C2}$

recall the $I_C - V_{BE}$ Relation: $I_C = I_S \cdot (e^{V_{BE}/V_T} - 1) \simeq I_S \cdot e^{V_{BE}/V_T}$ if $V_{BE} > 0$

where I_S: [reverse] saturation current , V_T: thermal voltage: 26 mV

25 mV

$\rightarrow I_{C1} = I_{S1} e^{V_{BE1}/V_T}$ & $I_{C2} = I_{S2} \cdot e^{V_{BE2}/V_T}$

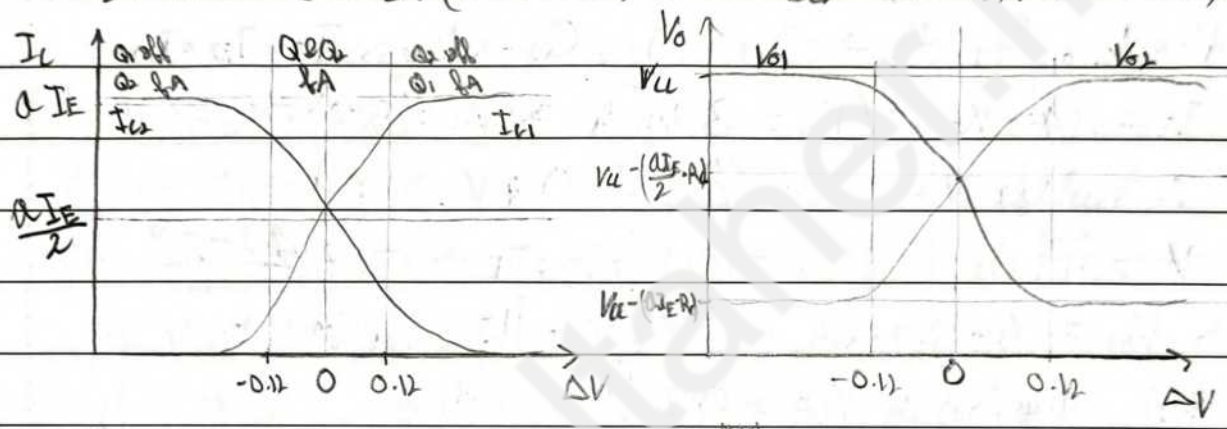
$\therefore V_{BE1} - V_{BE2} = V_1 - V_2 = \Delta V$

$\therefore \frac{I_{C1}}{I_{C2}} = \frac{I_{S1}}{I_{S2}} \cdot e^{(V_{BE1} - V_{BE2})/V_T}$ if $I_{S1} = I_{S2}$

$\rightarrow \frac{I_{C1}}{I_{C2}} = e^{(V_{BE1} - V_{BE2})/V_T}$

$\therefore \alpha I_E = I_{C2}(1 + e^{\Delta V/V_T})$ & $\alpha I_E = I_{C1}(1 + e^{-\Delta V/V_T})$

$\rightarrow I_{C1} = (\alpha \cdot I_E)/(1 + e^{-\Delta V/V_T})$ & $I_{C2} = (\alpha \cdot I_E)/(1 + e^{\Delta V/V_T})$

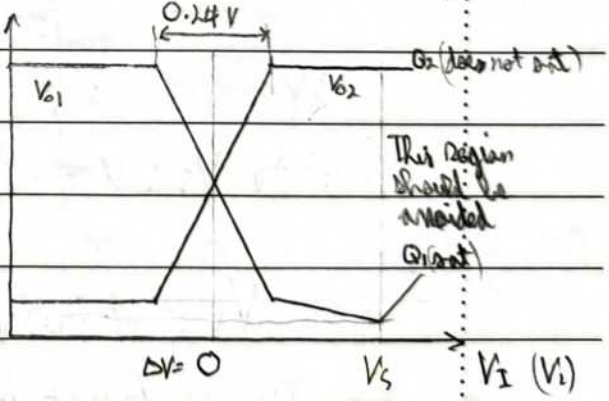


$\lim_{\Delta V \to -\infty} (I_{C2}) = \alpha I_{E2}$, if $|\Delta V| = 0.1$, $e^{-\frac{\Delta V}{V_T}} = 1$

- Hence, I_E is constant. as $I_{E1} \downarrow$, $I_{E2} \uparrow$ equally
- If the circuit shown below is to be operated as a logic element, then ΔV should always be smaller than -0.12 V or larger than 0.12 V as the region where $-0.12 < \Delta V < 0.12$ has both Q_1 and Q_2 on and outputs will be indeterminate. (circuit will operate as a diff amp)
- assuming V_2 is fixed and V_1 is V_I

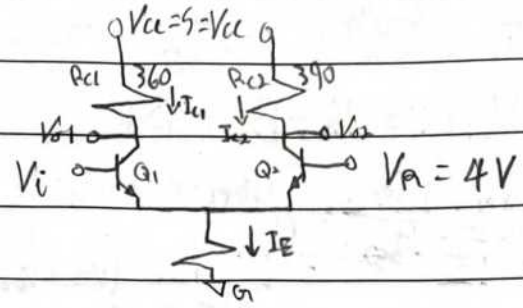
V_S: the voltage at which Q_2 saturates

$$V_S = V_I = \frac{V_{CC} + V_{BE1(sat)} + (V_{BE1(sat)} + V_{EE})\frac{R_{C1}}{R_E}}{1 + \frac{R_{C1}}{R_E}}$$



$V_{BE1(sat)} = V_{BE1(sat)} - V_{CE(sat)}$

* Basic ECL inverter/buffer:



- Remember the 0.24 V region in which both transistors are active must be avoided.

→ $V_{IL} < 3.88$, max $V_{IL} = 3.88V$ $V_R - 0.12$

→ $V_{IH} > 4.12$, min $V_{IH} = 4.12V$ $V_R + 0.12V$

- at $V_i = L$; Q_1 off → $I_{C1} = 0$, Q_2 active → $I_E = I_{E2} = I_{C2}$

$I_E = (4 - V_{BE(on)})/1k = 3.3\,mA$ → $V_{O2} = 5 - 3.3 \cdot 390 = 3.713 = \boxed{L}$

∴ buffer $V_{OL} \triangleq V_{EE} \simeq 0.4V$ → not bad

- at $V_i = H$: Q_2 off → $I_{C2} = 0$, $I_{C1} = I_{E1} = I_E$ → $I_E = \frac{4.2 - 0.9}{1k} = 3.3\,mA$

→ $V_{O1} = 5 - 360 \cdot 3.3 = 3.814V = \boxed{L}$, V_{O1} inverter

Check active/sat: $V_{CE} = 0.24V$ → active

- If $V_i = 5V = V_{CC}$:

assume Q_1 is on: $V_E = V_i - V_{BE(on)} = 5 - 0.9 = 4.3V$

$I_E = I_{C1} = \frac{4.3}{1k} = 4.3\,mA$, $V_{O1} = 5 - 0.36 \cdot 4.3 = 3.452V$ L

Check saturation: $V_{CE} = V_{O1} - V_E = -0.848V$ Sat. must: Redo calc.

Recalculate for sat: $V_E = V_i - V_{BE(sat)} = 4.2V$ → $I_E = 4.2\,mA$

∴ $V_{O1} = V_E + V_{CE\,sat} = 4.4V$

→ $I_{C1} = \frac{5 - 4.4}{360} = 1.667\,mA$

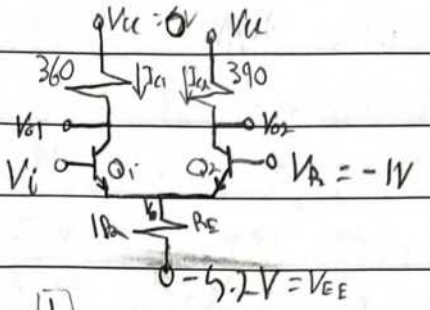
∴ $I_B = 2.533\,mA$

Calculate V_S: $V_i = \dfrac{V_{CC} + V_{BC(sat)} + (V_{BE,sat} + V_{EE})\frac{R_{C1}}{R_E}}{1 + \frac{R_{C1}}{R_E}}$

→ $V_i = 4.329V = V_S$

∴ max $V_{IH} = 4.329V$

* for $V_B = -1V$ & $V_{EE} = -5.2V$, $V_{cc} = 0V$



- if $V_i = L$, $V_i < -1.12V$:

Q_1 off, Q_2 on, $I_{C1} = 0$, $I_{C2} = I_E$

$I_E = \frac{-1 - 0.7 - (-5.2)}{1k\Omega} = 3.5\,mA$

$V_{O2} = 0 - 3.5 \cdot 390 = -1.365V = \boxed{L}$

Check active: $V_{CE} = -1.365 + 1.7 = 0.335V \rightarrow$ active

- if $V_i = H$, $V_i > -0.88V$: $V_i = -0.8V$

Q_1 is on, Q_2 is off, $V_E = -1.5V \rightarrow I_E = I_1 = \frac{3.7}{1k\Omega} = 3.7\,mA$

$\rightarrow V_{O1} = -1.332V = \boxed{L}$, check active: $V_{CE} = -1.332 - (-1.5) = 0.168V$

$V_{CE} < 0.1$ on

- if $V_i = 0V = \boxed{H}$:

Q_2 off, Q_1 active $\rightarrow V_E = -0.7V \rightarrow I_B = I_{C1} = \frac{4.5}{1k\Omega} = 4.5\,mA$

$\rightarrow V_{O1} = -1.62V = \boxed{L}$

Check if assumption that Q_1 is active is correct:

$V_{CE} = -1.62 - (-0.7) = -0.92V$

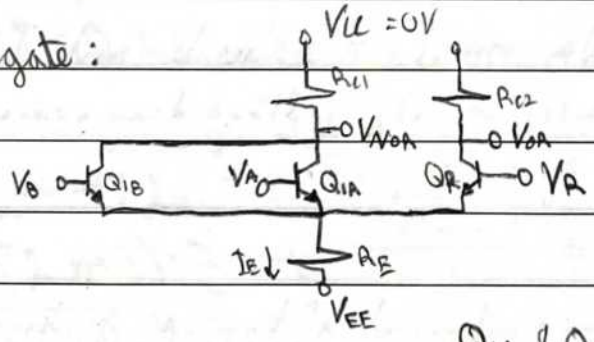
hence assumption is false and Q_1 is sat

$\rightarrow V_E = 0 - V_{BE(sat)} = \boxed{-0.8V}$, $I_E = \frac{4.4}{1k\Omega} = 4.4\,mA$

$\rightarrow V_{O1} = 0.2 - 0.8 = -0.6V \rightarrow I_{C1} = \frac{0 + 0.6}{360} = 1.667\,mA$

$\therefore I_{B1} = 2.733\,mA$

* Basic OR/NOR ECL gate:



- if V_A or V_B (or both) are high then their respective transistors will be forward active while Q_A will be off

$\rightarrow V_{NOR} = L$ $V_{OR} = H = V_{CC} = 0V$

Q_{1A} & Q_{2A} are in parallel

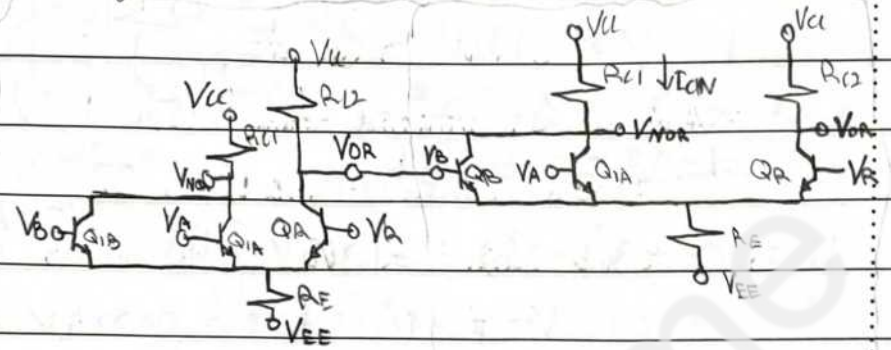
- if both V_A & V_B are low, Q_{1A} & Q_{1B} will be off, Q_A will be forward active

$V_{OR} = \boxed{L}$, $V_{NOR} = \boxed{H} = 0V = V_{CC}$

Subject Date No.

* fan-out of ECL OR/NOR gate: $V_{CC} = 0V$

- for an ECL OR/NOR gate supplying the input of another OR/NOR gate from its NOR terminal:



drives load

1) if $V_B = V_A = L \rightarrow V_{OR} = L$ next stage $V_B = L \rightarrow Q_B$ off hence an infinite number of gate can be driven

$N_L \rightarrow \infty$

2) if either V_A or V_B of the driver circuit is high (or both), Q_R will be off and $V_{OR} = V_{CC} - I_{C2} \cdot R_{C2}$

- if V_A of the second stage is low $\rightarrow Q_{1A}$ is off, I_{CIN} passes completely through Q_{1B}, which gives the output of the emitter of the load $Q_R = I_{BB} + I_{CIN}$, where I_{BB} is the total current I_{C2} of the driver divided by the N loads.

- if V_A is high, the current I_{CIN} will be divided evenly among Q_{1B} and Q_{1A}, giving $I_{EBN} = I_{BB} + \frac{I_{CIN}}{2}$

Q_R must not saturate and I_{C2} must not get large enough to cause the voltage drop across R_{C2} to reduce V_{OR} from high to low.

to be continued after quiz practice and quiz

Subject Quiz two practice Date 10/4/2021 No.

P1.2: $V_i = 0.1V \Rightarrow V_{B1} = 0.9 \Rightarrow I_B = 0.82\,mA$

$V_{B2} = V_{C1} = 0.3V \Rightarrow Q_2$ off, Q_3 off $\Rightarrow I_{C3} = 0 = I_{C2}$

$V_i = 4V \Rightarrow Q_1$ Reverse active, Q_2 sat $\Rightarrow V_{B2} = 0.8V$ ×

$\Rightarrow V_{B1} = 0.8 + V_{BE(sat)} = 1.4V \Rightarrow I_1 = 0.72\,mA$ ×

Q_3 sat as well $\Rightarrow V_{B3} = 0.8V \Rightarrow V_{B2} = 1.6V$

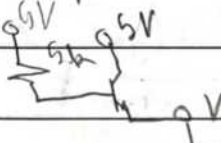
$\Rightarrow V_{B1} = 2.2V \Rightarrow I_1 = 0.56\,mA$

$\because Q_2$ sat $\Rightarrow V_{C2} = 0.2 + 0.8 = 1V \Rightarrow I_2 = 1.6\,mA$

$\wedge V_o = 0.2V \Rightarrow I_3 = 2.4\,mA$

total power supply current = $4.56\,mA$

Q2:



$-5 + 5k \cdot I_B + 0.7 + I_E \cdot 1k = 0$

$I_E = (1+\beta_1) \cdot I_B$ ∧ $\beta = 50 \Rightarrow I_B(5k + 51 \cdot 1k) = 4.3$

$\Rightarrow I_B = 76.78\,\mu A$

$\Rightarrow V_o = 76.78 \cdot 51 \cdot 1k = 3.9161$ not sat

$= 3.92V$

Q3: Q_1 Rev active, Q_2 sat Q_3 sat $\Rightarrow V_{B3} = 0.8V$, $V_{B2} = 1.6V$

$V_{B1} = 2.2V$

$\because Q_3$ sat $\Rightarrow V_o = 0.2V$

3 gates connected Q_{1N} sat $\Rightarrow V_{B1N} = 0.9V$ × 1V

$\Rightarrow I_{E1N} = \frac{4.1}{5k} = 0.82\,mA$ × 0.8 mA

$\Rightarrow I_{C1} = (0.82\,mA) \cdot 3 + \frac{5 - 0.2}{2k} = 4.86\,mA$

0.8 mA · 3 + // = 4.8 mA

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Q4: $V_o = 0.2V$ X

$I_{C1} = \frac{5-0.2}{2k} + 2\left(\frac{5-(0.2+0.8)}{4k}\right)$ X X

Q_1 sat & input low → Q_2 cut → $V_o = V_{CC}$

V_o input to two gates

Q_{1N} reverse active → Q_2 & sat → $V_{BIN} = 1.4V$

→ $I_{BIN} = 0.9\,mA$ $\beta_{R1} = 0.2$

→ $I_{EIN} = 0.18\,mA$

→ ~~I_{CIN}~~ = $I_{C1} = 0.18 \cdot 2 = 0.36$

∴ $V_o = 5 - 0.36 \cdot 2k = \boxed{4.28\,V}$

& H → L input

$I_{B1} = \frac{5-0.9}{4k} + I_{C1} = \frac{5-0.9}{4k} + 51 \cdot \frac{5-0.9}{4k} = 53.33\,mA$

$I_{C1} = (\beta_F+1) I_B$ & $I_B = \frac{5-0.9}{4k}$

$I_{B1} = \frac{V_{CC} - V_{BE}}{R_1}$ & $V_{BE} = 0.2+0.9+0.8 = 1.9$

→ $I_{B1} = 3.3/1.6k = 2.0625\,mA$

$I_{C1} = \frac{V_{CC} - V_C}{130}$ $V_C = 0.2+0.9+0.2 = 1.1$

→ $I_{C1} = \frac{3.9}{130} = 0.30\,mA$

→ I_{E1} ~~changing~~ = $30 + 2.0625 = 32.0625$

Q5: Q_1 low → $V_{B1} = 0.9$ $I_{B1} = \frac{4.1}{4k} = 1.025\,mA$

→ $I_{E1} = (\beta+1) \cdot I_{B1} = 59.4\,mA$

→ $I_{C1} = I_{B2} = \beta \cdot I_{B1} = 56.375\,mA$ outside base

P3: $V_A = 4V$ → Q_1 in Rev. active, Q_3 & Q_2 sat

→ $V_{BE1} = 1.6V$ → $V_{B1} = 2.2V$ → $I_{B1} = 0.56mA$

→ $I_{C1} = 0.56 \cdot (1+0.1) = 0.616\,mA$

& Q_2 sat → $I_{C1} = \frac{5-1}{2.5} = 1.6\,mA$

→ $I_{E2} = 2.216\,mA$

$I_{B3} = I_{E2} - 0.8/1k = 1.416$

P4:  Q_2 ~~sat~~ → X no current since $R_L = \infty$

$V_{BE_{ON}} = 0.7V \rightarrow V_o = 5 - 0.6 = 4.4V$

P5: Q_2 cutoff → Q_1 in active → $I_{BIN} = \frac{3.6}{4k} \rightarrow I_{EIN} = 0.18mA$

$\therefore I_{RL} = 0.18\,mA \quad V_o = 4.64V$

Quiz 2:

1) Q_2 sat → $V_o = 0.2V$

$\beta I_B \sigma = I_C$

$I_B = \left(\frac{5-1.4}{4k}\right)/(1+0.11) = 0.999\,mA$

$I_C = \frac{4.8}{1k} + 8.1mA = 10.4$

$10.4 = 0.999 \cdot 42 \cdot \sigma \rightarrow \boxed{\sigma = 0.24986}$

2) $V_{B1} = 2.2 \rightarrow I_{B1} = 0.46\,mA$

$V_o = 0.2\,mA$

$0.8\,mA \cdot 5 = 4\,mA$

$= 1.4$

3) Q_2 & Q_3 sat → $V_o = 0.2V$

$12 \cdot 1 = 12\,mA$

$\frac{5-1.7}{1.6k} =$

4) $5 \cdot 1 = 5\,mW$ → $Q_1 P$

$\frac{5-1.4}{4k} = \boxed{0.9} \times 3$ → I_{BIN}

$0.18 = \beta_{DEV}$

$I_{EIN} = I_{BIN} \cdot \beta_{DEV} = \boxed{0.162\,mA}$

If we calculate power consumed for a single circuit

$\therefore I_{C2} = 0.162 \cdot 3 = 0.486\,mA$

$\therefore Q_2 P = 5 \cdot 0.486 = 2.43\,mA$

$\rightarrow P_{total} = \boxed{7.43\,mW}$

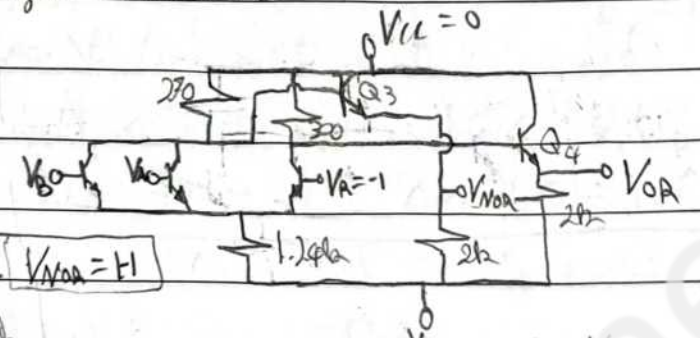
* modified OR/NOR ECL gate: MECL I

Q_3 and Q_4 are always forward active

If Q_R is forward active

→ Q_A ∧ Q_B off → $V_A = V_B = L$ $V_{NOR} = H$

If Q_R is off, Q_A or Q_B or both are forward active $V_{OR} = H$



1) If V_A and V_B are low:

$0 + 270 \cdot I_{B4} + 0.7 + I_{E4} \cdot 2k - 5.2 = 0$ ∧ $I_{E4} = (\beta+1) I_{B4}$

→ $I_{B4}[270 + (\beta+1) \cdot 2k] = 5.2 - 0.7$

If $\beta = 100$ → $I_{B4} = 22.25\,\mu A$ → $V_{NOR} \simeq -0.7V = H$

∧ $I_{BC2} - I_{B4} = I_E = \frac{-1.4 - -5.2}{1.24k} = 2.82258$

∧ $0 + I_{BC2} \cdot 300 + 0.7 + I_{E4} \cdot 2k - 5.2 = 0$

→ $(2.82258 + I_{B4}) \cdot 300 + 0.7 - 5.2 + (\beta+1) I_{B4} \cdot 2k = 0$

→ $I_{B4}(300 + (\beta+1)2k) = 3.653226$, $\beta = 100$

→ $I_{B4} = 18.058\,\mu A$ → $V_{OR} = -1.6522\,V = L$

2) If V_A and/or V_B are high:

$V_A = V_B = H = -0.7V$ → $V_E = -1.4$ → $I_E = I_{EA} + I_{EB} = \frac{-1.4 - -5.2}{1.24k} = 3.06452\,mA$

→ $V_{NOR} = -3.06452\,m \cdot 270 - 0.7 = -1.527 = L = V_{NOR}$

∴ Q_R off ∧ V_{BC2} negligible → $V_{OR} = -0.7V = H$

∴ $V_A = -1$ → $V_{IH} = -0.88$ ∧ $V_{IL} = -1.12$

∧ NOR: $V_{OH} = -0.7V$ ∧ $V_{OL} = -1.528\,V$

OR: $V_{OH} = -0.7V$ ∧ $V_{OL} = -1.65V$

∴ noise margins: OR: $NM_H = 0.18V$ ∧ $NM_L = 0.43$

NOR: $NM_H = 0.18V$ ∧ $NM_L = 0.408$

Subject mid exam practice (+ forward ECL) Date 12/4/2021 No.

* modified OR/NOR ECL gate : MECL1 fan-out

if V_A ∧ V_B are high, OR output will be high and OR off

$I_{E4} = I_{RE4} + N \cdot I_{load}$ assume Q_{1A} : inactive

assuming $V_{OR} = -0.75V$ ∧ $I_{E1} = I_{BE1} = I_{load} + I_{C1}$

∧ $+0.75 + 0.7 + 1.24k \cdot I_{E1} - 5.2 = 0$

→ $I_{E1} = 3.0242\ mA$ $= (\beta+1) \cdot I_B$

∴ $I_B = I_1$ ∧ $\beta = 100$ → $I_1 = 29.9426\ \mu A$

∴ $I_{E4} = (\beta+1) I_{B4} = I_{RE4} + N I_1$

∧ $I_{RE4} = \frac{-0.75 - -5.2}{2k} = 2.225\ mA$ ∧ $I_{B4} \cdot 300 + 0.7 - 0.75 = 0$ → $I_{B4} = 0.1667\ mA$

∴ $(\beta+1) \cdot 0.16667m = 2.225m + N \cdot 29.943\mu$

→ $N = \frac{14.608}{0.0299} = 488$ fan-out for high output logic

* modified 2:

$V_B = 0.7 + 0.7 + I_{R2} \cdot 2.3k - 5.2$

∧ $V_B = 0.7 + I_{E5} \cdot 2k$ $I_{E5} = \beta_{NPN} I_{BS}$ assume $I_{BS} = 0$ negligible

→ $0.7 + I_{R2} \cdot 2.3k - 5.2 = (\beta+1) I_{BS} = (\beta+1)(I_{R1} - I_{R2})$

∧ $I_{R1} \cdot 300 + 0.7 + 0.7 + I_{R2} \cdot 2.3k - 5.2 = 0$

→ $I_{R1} = \frac{5.2 - 1.4 - I_{R2} \cdot 2.3k}{300}$

→ $-4.5 + I_{R2} \cdot 2.3k = 101 \cdot \left(\frac{3.8}{300} - I_{R2}\left(\frac{2.3k}{0.3k} + 1\right)\right)$

→ $I_{R2} \cdot 2.3k = 4.5 + 1.27933 - 875.333 \cdot I_{R2}$

→ $I_{R2}(2300 + 875.333) = 4.5 + 1.27933333$

→ $I_{R2} = 1.82\ mA$ → $I_{R1} = -$

→ $0 + 300 I_{R1} + 0.7 + 0.7 + 2.3 I_{R2} = 5.2$, $I_{R1} = I_{R2}$

→ $I_{R1} = 1.462\ mA$

∧ $V_B = -0.437k$ ∧ $V_A = V_B - V_{BE(on)} = -1.137k \simeq -1.14V$

quiz 1 redone:

1) $NM_H = 3V \Rightarrow V_{OH} - V_{IH} = 3V$

$NM_L = V_{IL} - V_{OL}$ $\because V_{OH} = V_{CC} = 5V$

$\rightarrow V_{IH} = 5-3 = 2V$ $\because -2 + I_B R_B + 0.8 = 0$

$\wedge -5 + I_C R_C + 0.2 = 0$

$\rightarrow I_C = \frac{4.8}{2k} = 2.4mA$

assume EOS: $\sigma I_B \beta = I_C$, $\sigma = 1 \rightarrow I_C = \beta I_B$

$\rightarrow I_B = 24.8\mu A \rightarrow \beta = 48.3$

2) $\sigma I_B \beta = I_C \rightarrow \sigma = \frac{I_C}{I_B \beta}$, $I_C = 0$ if $V_O = H$

$\rightarrow I_C = \frac{5-0.2}{4k} = 1.2mA$

$\wedge I_B = I_{D1} - \frac{0.8}{5k}$

$\wedge I_{D1} = I_{B1}$ $\because V_A \wedge V_B$ high

$V_P = 0.8 + 0.7 + 0.7 = 2.2V \rightarrow I_{D1} = 1.3461538mA$

$\rightarrow I_B = 1.1861538\mu A \rightarrow \sigma = 0.015516$

Q3: $\sigma = 0.9 = \frac{I_C}{I_B \beta}$ $\wedge I_C = \frac{5-0.2}{1k} = 4.8mA$

$\rightarrow I_B = 0.106667mA$ $\wedge I_B = \frac{V_i - 0.8}{13.1k} \rightarrow V_i = 2.19733V$

Q4: $I_C = 0$ if $V_A \wedge V_B$ high

$\rightarrow I_C = \frac{V_{CC} - V_O}{4k} + \frac{5-0.9}{2.42k} = \frac{4.8}{4k} + \frac{4.1}{2.42k} \cdot \frac{1}{2}$ since other input low

Q5: Q_1 cutoff, assume gates are not $\Rightarrow$

$-V_{CC} + R_C \cdot N I_B + V_O = 0$

$\wedge -V_O + I_B \cdot \beta_B + 0.8 = 0 \rightarrow V_O = I_B \cdot R_B + 0.8$

$\rightarrow -V_{CC} + I_B(N \cdot R_C + R_B) + 0.8 = 0$

$\rightarrow I_B = 223.4\mu A$

$\rightarrow V_O = 3.66V$

first 5 17-18:

P1: Assume EOS, $V_{IH} \to V_{OL}$

$V_{OL} = 0.2V \to I_{B1} = \frac{5-0.2}{1k} = 4.8mA$

inputs tied together $\to \frac{4.8mA}{2} = I_C = 2.4mA$

∴ EOS $\to \sigma \cdot \beta I_B = I_C$ ∧ $\sigma = 1 \to I_B = \frac{2.4}{20} = 0.12mA$

∧ $V_{IH} = 0.8 + 0.12m \cdot 15k = 2.6V$

2) for high logic:

$-5 + NI_B \cdot 1k + I_B \cdot 15k + 0.8 = 0$

∧ $V_{O\,min\,H} = V_{IH} \to V_O = 5 - 1k \cdot NI_B = 2.6V$

noise margin $\to V_{IL} < V_{OH} < V_{IH}$

$\to N \cdot I_B = 2.4mA$

∴ $-5 + 2.4 + I_B \cdot 15k + 0.8 = 0 \to I_B = 0.12$

$\to N = 20$

P2) 1) $V_A = V_B = 0.1V \to V_O = 0.8V \to I_{D1} = \frac{4.2}{4k} = 1.05mA$

$\to I_{DA} = 0.525mA$ ∧ $I_{D2} = 0$ ∴ D_1 is ON

2) $0.8 \cdot \beta \cdot I_B = I_C$, $V_O = 0.2V \to I_C = 1.2mA$

$V_{B1} = 2.3V \to I_{B1} = \frac{5-2.3}{4k} + \frac{5-1.7}{2k} = 2.325mA$

$\to I_{B2} = 2.325 - \frac{0.8}{4k} = 2.125mA$

∴ $0.8 \cdot 2.125m \cdot \beta = 1.2m \to \beta = 0.682$

3) If $V_A = V_B = 5V \to P_D = 5(0.675 + 1.65 + 1.2)m = 17.625mW$

4) for a load output: $I_C = N \cdot \left(\frac{5-0.9}{4k}\right) + \frac{5-0.2}{4k}$

EOS $I_C = \beta I_B = 120 \cdot 2.125m$

$\to \boxed{N = 42}$

P3: 1) Q_1 reverse active, $Q_3 = Q_2 =$ sat $\rightarrow V_{B2} = 1.6V$

$\therefore I_{B1} = \frac{5 - 1.6 - 0.6}{6k} = 0.46667\,mA \rightarrow I_{C1} = I_{B2} = 0.5133\,mA$

$\Lambda\ I_{B3} = I_{E2} - \frac{0.8}{1.5k}$ $\Lambda\ I_{E2} = 0.5133m + \frac{4}{2k}$

$\rightarrow I_{B3} = 1.97999...\,mA$

2) if $V_{x1} = 0.3V$, Q_1 sat $\rightarrow V_{B1} = 1.1V \rightarrow$

Q_2 on, Q_3 off, Q_4 forward active:

$-5 + I_{B4} \cdot 2k + 0.7 + 0.7 + (1+\beta) I_{B4} \cdot 1k = 0$

$\rightarrow I_{B4} = 0.1565\,mA \rightarrow V_o = 3.287\,V$

3) $-5 + I_{B4} \cdot 2k + 1.4 + 10 I_{B4} \cdot 1k = 0$

$\rightarrow I_{B4} = \frac{3.6}{12k} = 0.2916667\,mA$

$\rightarrow V_o = 2.416667\,V \rightarrow V_{E4} = 3.616667\,V$

$\Lambda\ V_C = 5 - 80 \cdot I_B \cdot 80 = 4.79\,V$

$\rightarrow V_{CE} = 1.17$

4) low-output: $I_{B3} \approx 2mA$

KCL $\rightarrow$ $1.2m = I_C$ $\Lambda\ I_C = N \cdot I_{E1}$

$\Lambda\ I_{E1} = \frac{5 - 0.9}{6k} \rightarrow N = 26$

* ECL positive:

P1: $V_R = 0$

a) $V_i = 0 \rightarrow I_E = \frac{3.3}{450} = 7.33\,mA$

$\rightarrow I_{E1} = I_{E2} = \frac{7.33}{2} = 3.6667\,mA$

$\rightarrow I_{C1} = I_{C2}$

b) $V_i = -0.1V$ $\because V_i < V_R \rightarrow Q_1$ off, $V_{o1} = 2V$

Q_2 on $\rightarrow I_E\ I_{E2} = 7.333\,mA$ $\Lambda\ I_{C2} = 7.26\,mA$

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Mid practice:

2) $V_A = \frac{V_{OL} + V_{OH}}{2}$ Q0 fA

$V_0 = 0 + I_{B1} \cdot 0.3k + 0.7 + I_{E0} \cdot 2k - 5 = 0$

$\Rightarrow V_{OH} = -0.7V$

$\wedge$ $V_{OL} \rightarrow V_x$ on V_B on $\Rightarrow I_C = \frac{(V_A + 0.12) - 0.7 - -5}{1.2k}$

$\Rightarrow V_{OL} = 0.3k \cdot \frac{4.3 + V_A + 0.12}{1.2k} + 0.7 - 5$

on assume $V_x = 0 \Rightarrow I_C = \frac{-0.7 - -5}{1.2k} = 3.468\ mA$

$\Rightarrow V_{OL} = -1.7403 \Rightarrow V_B = -1.22 \times$

$I_E = +2.903\ mA = I_C \Rightarrow V_{OL} = -1.5709$

$\Rightarrow V_B = -1.135V$

4) $V_{IH} = 4.75 + 0.12 = 4.87\ V$ $\wedge$ $V_{OH} = V_{cc} = 5V$

$\rightarrow NM_H = 0.13$

5) $V_x = V_y = H$, Q... $\Rightarrow I_E = \frac{5 - 0.85 - 0.7}{1.2k}$

$\Rightarrow I_E = 2.78225\ mA \Rightarrow I_{Cx} = I_{Cy} = \frac{I_E}{2} = 1.39\ mA$

6) Qx is sat., $I_E = \frac{5 - 0.8}{1.3k} = 3.23077\ mA$

$\Rightarrow V_0 = 5 - 3.23077 \cdot 0.3 = 4.0311\ V$

$NM_L = V_{IL} - V_{OL}$

$NM_H = V_{OH} - V_{IH}$

2) $V_{OH} = 0$, $V_{OL} = -1.7403 \Rightarrow V_A =$

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1) Q_3 off, Q_1 off $\quad -5 + I_{B2} \cdot 5k + 0.7 + (1+\beta) I_{B2} \cdot 1k = 0$

$\rightarrow I_{B2} = \frac{5 - 0.7}{(1+\beta)1k + 5k} = 71.6669\,\mu A$

$\rightarrow V_0 = 3.94$

2) $V_A = V_B = H \rightarrow Q_1$ sat $\wedge$ Q_2 sat.

$\rightarrow V_{B2} = 2.3 \rightarrow I_{B1} = \frac{5 - 2.3}{38k} = \frac{2.7}{38k}$

$I_{B2} = I_{E1} - \frac{0.8}{2k}$

$I_{E1} = \frac{2.7}{38k} + \frac{3.3}{2k} \rightarrow I_{B2} = 1.32$

3) $V_{BE_{on}} = 0.7$

Q_X off

$5 - 0.3 \cdot I_C = V_0$

$I_E = I_B + I_C$

$I_E = (1+\beta) I_B$

$-5 + 101 I_B \cdot 0.3 + 0.7 + I_B(1+\beta) \cdot 1.3 = 0$

$\rightarrow I_B = \frac{4.3}{101 \cdot 0.3 + (1+\beta) \cdot 1.3} = 76.11\,A$

$V_0 = 5 - 15 \cdot I_B \cdot 0.3 = 4.6575$

4) Q_1 on Q_3 off:

$Q_1 \wedge Q_3$ sat $\rightarrow -V_i + I_{B1} \cdot 4k + 0.8 = 0$

$\wedge -V_i + I_{B3} \cdot 10k + 0.8 = 0$

$-5 + 5k \cdot I_{B6} + 0.7 = V_i$

$I_{B3} + I_{B1} = I_{B6}(1+\beta)$

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6) $V_A = V_B = 5V \rightarrow Q_1$ is Ron. sat.
Q_2 sat Q_3 sat
$V_o = L$
Q_2

7) V_{OH} $V_{OH} = 3.6$
$V_{IH} \Rightarrow -V_{IH} + I_B \cdot R_B + 0.8 = 0$
$V_{IH} = I_B \cdot R_B - 0.8$
EOS $= I_B \cdot \beta = I_C \rightarrow I_C = \frac{1}{2} \frac{3.6 - 0.2}{4k\Omega}$

$\rightarrow I_B = 75\,\mu A \rightarrow V_{IH} = 0.8489$

8) $V_x = V_H$ active
$I_E = -0.76 - 0.7 + 5 / 1.04k = 2.855\,mA$
$\rightarrow I_{E4} = \frac{1}{2} I_E = 1.421$

9) Q_1 Ron active
$I_{C2} = \frac{V_a - 0.2}{2k} + 7 \cdot 1mA = 1.4\,mA$

10) $V_A = V_B = H$
$V_P = 2.2V \rightarrow I_{D1} = 1.34\,mA$
$\rightarrow I_B = 1.18\,mA$
$\sigma = 59.1 \cdot 1.18 = I_C$, $I_C = \frac{5 - 0.2}{4k} = 1.2mA$
$\rightarrow \sigma = 0.01721$

11) $\frac{P_H + P_L}{2}$ $P_H = 0$

$P_L = 3.6 \cdot \frac{3.4}{4.99} = 26.78\,mA$

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12) put at base

13) 0.9 $\frac{5-0.4}{1k} \cdot 93 = 43.46$ out

14) $\sigma = \frac{I_C}{\beta I_B}$

$-4.1 + I_{B1} \cdot R_B + 0.8 + 0.2 = 0 \rightarrow I_{B1} = 0.3541\,mA$

$V_o = 0.4 \rightarrow I_{CA} = \frac{5-0.4}{1k} = 4.6mA$

$\rightarrow \sigma = 0.362$

15) V_A high $\rightarrow V_o = L \quad I_C = \frac{4}{5k} \cdot 6 = 4.8\,mA$

$\wedge I_{B3} = I_{E2} - \frac{0.8}{1k} \quad \wedge I_{E2} = \frac{4}{2.2k} + (1+\beta_{Rev})\,0.56$

$\rightarrow I_{E2} = 2.216\,mA \rightarrow I_{B3} = 1.416\,mA$

$\rightarrow \sigma =$

$I_C = 4.8 + \frac{5-0.2}{2k} = 7.2\,mA$

$V_o = L = 0.2 \rightarrow I_C = \frac{5-0.2}{2k} + 6 \cdot \frac{4}{5} = 7.2mA$

$\wedge I_B = I_{E2} - 0.8mA \quad I_{E2} = \frac{4}{2.5} + \frac{2.8}{5} \cdot 1.1$

$\rightarrow I_{E2} = 2.216 \rightarrow I_{B3} = 1.416mA$

$\sigma =$

$\frac{4}{5k} \cdot 5 + \frac{5-0.2}{2k} = 6.4\,mA$ (1.344)

$I_{B2} = 1.1 \cdot \frac{5-2.2}{5k} = 0.616$

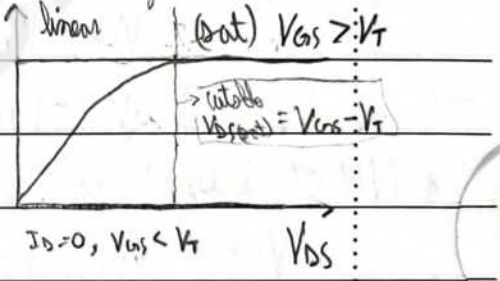
$0.616 + \frac{5-1}{2.5k} = 2.216\,mA \rightarrow I_{B2} = 1.416$

$\rightarrow \sigma = \frac{6.4}{50 \cdot 1.416}$

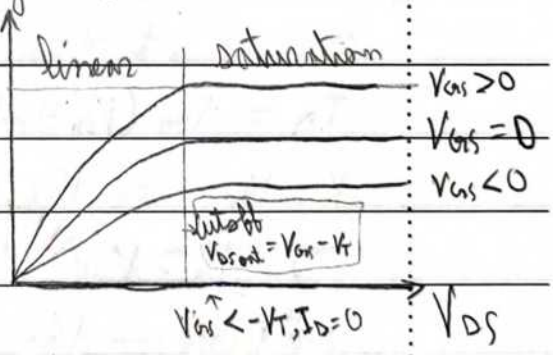
Subject Chapter 7: NMOS logic Date 24/4/2021 No.

* MOSFET: N-channel or P-channel
  - subcategory: enhancement or depletion (simplified to single letter)
    → NMOS: E-NMOS ∧ D-NMOS | PMOS: E-PMOS ∧ D-PMOS
- depletion type (D-NMOSFET) is normally on, whereas enhancement mode (E-NMOSFET) is normally off
- depletion type has a built in channel whereas enhancement type must create it
- the V_{GS} required to create the channel is called the threshold voltage (V_T) and is positive for E-NMOS and negative for D-NMOS.

E-NMOSFET IV characteristics

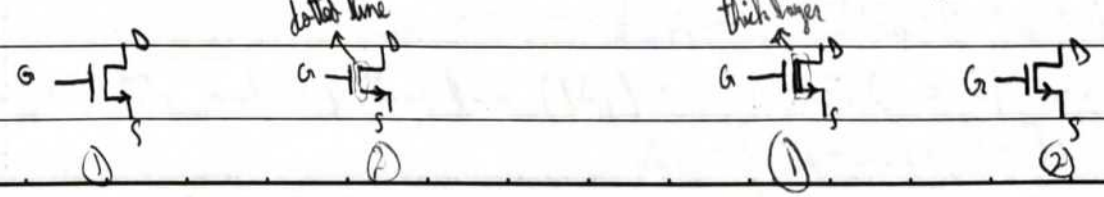


- for D-NMOS, the required V_{GS} to deplete the channel is the threshold voltage (V_T) and is negative
- an oxide separates the gate from the p-substrate (which separates the source and drain). The thickness of this oxide layer is (t_{ox}).



* symbols for enhancement type NMOSFETs and corresponding symbols for depletion type

enhancement type: depletion type



either (1) or (2) will be consistently used.

* three modes of operation of the NMOS:

1- cutoff:

$V_{GS} < V_{TN}$, $I_D = 0$ for enhancement: $V_{GS} > 0$

2- saturation:

$V_{GS} > V_{TN}$

$V_{DS} > V_{GS} - V_{TN}$

$I_D = k_n (V_{GS} - V_{TN})^2$

V_{TN}: threshold voltage

k_n: channel conduction parameter, $k_n = \frac{W}{L} \frac{\mu_n C_{ox}}{2}$

W & L: channel length and width, C_{ox}: capacitance of oxide per unit area

The main two parameters of a MOSFET are V_T & k_n

3- ohmic (linear):

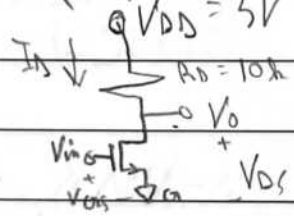
$V_{GS} > V_{TN}$

$V_{DS} < V_{GS} - V_{TN}$

$I_D = k_n [2(V_{GS} - V_{TN}) V_{DS} - V_{DS}^2]$

* NMOS inverter with resistive load:

R_D is the pulling network



$V_{TN} = 1V$, $k_n = 100 \mu A/V^2$

$R_D \cdot k_n = 1 V^{-1}$

$V_{GS} = V_{in}$ & $V_o = V_{DD} - I_D \cdot R_D$

+ if $V_{GS} < V_{TN}$: $I_D = 0$ & $V_o = V_{DD} = 5V$

+ if $V_{in} > V_{TN}$:

- assume sat then check assumption:

$I_D = k_n (V_{in} - V_{TN})^2$

$V_o = V_{DS} = V_{DD} - [k_n (V_{in} - V_{TN})^2] \cdot R_D > V_{in} - V_{TN}$ (for sat)

$\rightarrow V_o = V_{DS} = 5 - (V_{in} - 1)^2 > V_{in} - 1$

solving $V_{DD} - k_n R_D [V_{GS} - V_{TN}]^2 = V_{GS} - V_{TN}$

for $V_{GS} = V_{in} = V_s$

$\rightarrow$

$$V_s = V_{TN} - \frac{1}{2 k_n R_D} \pm \sqrt{\left(\frac{1}{2 k_n R_D}\right)^2 + \frac{V_{DD}}{k_n R_D}}$$

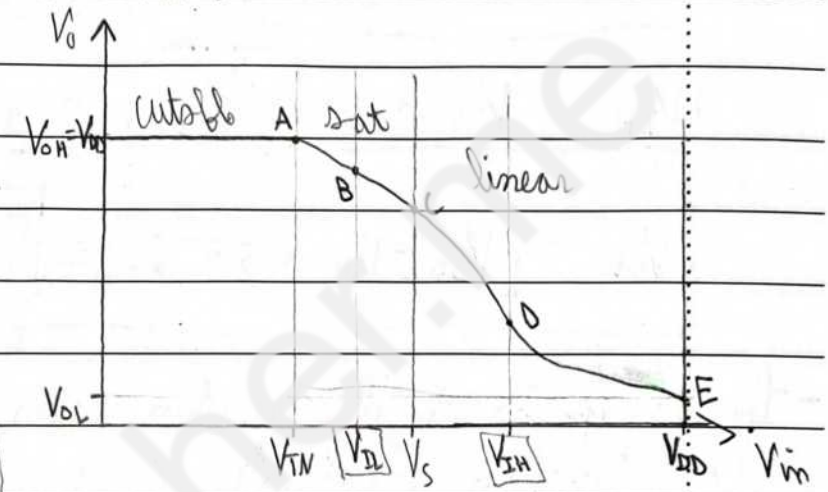
$\rightarrow V_s = 2.79 V$

- assume linear:

$$I_D = k_n\left[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2\right]$$

$$\rightarrow V_o = V_{DD} - R_D k_n\left[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2\right]$$

$$\therefore V_o = 5 - \left[2(V_{GS} - 1)V_{DS} - V_{DS}^2\right]$$



- point A: $V_{in} = V_{TN}$ and transistor leaves cutoff. (output before is high)
- point B: $\frac{dV_o}{dV_{in}} = -1$ (gain), here the input voltage is maximum low (any voltage level below is low).
- point C: The device leaves sat and enters linear mode
- point D: $\frac{dV_o}{dV_{in}} = -1$, voltages larger than V_{in} at this point will be high
- point E: the output at this point is low, $V_{input} = V_{DD} = V_{SH}$

+ to calculate input voltage low (V_{IL}):

$$\frac{dV_o}{dV_{in}} = -1 = -2R_D k_n(V_{in} - V_T)$$

$$\rightarrow \boxed{V_{in} = \frac{1}{2R_D k_n} + V_{TN}}$$

$$\wedge \boxed{V_o = V_{DD} - \frac{1}{4R_D k_n}}$$

+ to calculate input voltage high (V_{IH}):

V_o at D: $V_o = \sqrt{\frac{V_{DD}}{3R_D k_n}}$

$$\rightarrow V_{IH} = \frac{2}{\sqrt{3}}\sqrt{V_{DD} \cdot R_D k_n} + V_{TN} \cdot R_D k_n - \frac{1}{2}$$

+ to calculate output voltage low (V_{OL}):

$$V_{OL} = \left[(V_{DD} - V_{TN}) + \frac{1}{2R_D k_n}\right] \pm \sqrt{\left[(V_{DD} - V_{TN}) + \frac{1}{2R_D k_n}\right]^2 - \frac{V_o}{2R_D}}$$

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∴ for a resistive load inverter:

$$V_{OH} = V_{DD}$$

$$V_{IL} = V_{TN} + \frac{1}{2 R_D k_n}$$

$$V_{IH} = V_{TN} + 2\sqrt{\frac{V_{DD}}{3 R_D k_n} - \frac{1}{2 R_D k_n}}$$

$$V_{OL} = \left[V_{DD} - V_{TN} + \frac{1}{2 R_D k_n}\right] \pm \sqrt{\left[V_{DD} - V_{TN} + \frac{1}{2 R_D k_n}\right]^2 - \frac{V_{DD}}{R_D k_n}}$$

- the sharpness of the transition region increases with increasing R_D (as $R_D \cdot k_n$ increases)
- the minimum output voltage (the logic zero level) for a high input decreases with increasing R_D.
  (V_{OL} decreases as $R_D \cdot k_n$ increases)
- hence the inverter approaches ideal as R_D increases.
  (limit $R_D \cdot k_n \to \infty$)
- power dissipation: $P_D = \frac{V_{DD}}{2}\left[I_D(V_{in} = V_{OL}) + I_D(V_{in} = V_{OH})\right]$

for inverter with resistive load: $P_D = \left[\frac{V_{DD}}{2}\right] \cdot \left[\frac{V_{DD} - V_{OL}}{R_D}\right]$

* Steps to solving:

1- check V_{GS}, if $V_{GS} > V_T$ then transistor on. else off

2- check V_{DS}. if $V_{DS} > V_{GS} - V_T$, then saturated
   else if $V_{DS} < V_{GS} - V_T$, then linear active

3- if V_{DS} can't be checked first, assume sat then check if assumption is correct.

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design example: $k_n = 150\ \mu A/V^2$, $V_{TN} = 0.5V$

a) R_D for $V_o = 0.1V$ when $V_i = 3V$

∴ linear → $V_o = V_{DD} - R_D \cdot k_n [2(3-0.5)\cdot 0.1 - 0.1^2]$

→ $0.1 = 3 - R_D \cdot 150\mu [0.49]$ → $R_D = \frac{2.9}{7.35\times 10^{-5}} = 39.5k\Omega$

b) transition point: $V_o = V_s - V_{TN}$ sat

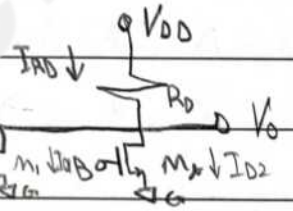
→ $V_{DD} - 39.5k \cdot 150\mu [V_s - \frac{1}{2}]^2 = V_s - \frac{1}{2}$

define: $x = V_s - \frac{1}{2}$ → $39.5k \cdot 150\mu \cdot x^2 + x - V_{DD} = 0$

→ $x = 0.63217$ or -0.809

→ $V_s = 1.13217\ V$

* NMOS NOR with resistive load:



- transistors do not saturate

A	B	V_o	M_1	M_2	
0	0	V_{DD}	off	off	$V_o = V_{DD} - I_{RD} R_D$
0	1	V_{DS1}	off	linear	$V_o = V_{DS1} = V_{DS2}$
1	0	V_{DS2}	linear	off	
1	1	V_{DS1}	linear	linear	

∴ $I_{D1} = k_{n1} V_{DS1} [2(V_{GS1} - V_{T1}) - V_{DS1}]$ & $I_{RD} = \frac{V_{DD} - V_o}{R_D} = I_{D1} + I_{D2}$

for $A = B$, $I_{D1} = I_{D2}$ → $I_{RD} = m \cdot I_{D1}$, m: number of transistors (here $m = 2$)

→ $\frac{V_{DD} - V_o}{R_D} = m k_n V_o [2(A - V_{T1}) - V_o]$, A = voltage input at A

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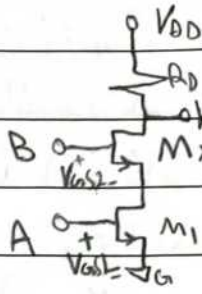
* NMOS NAND with resistive load:

A	B	V_o (logic)	V_o (V)	M_1	M_2
0	0	1	V_{DD}	off	off
0	1	1	V_{DD}	off	linear
1	0	1	V_{DD}	linear	off
1	1	0	$V_{DS1}+V_{DS2}$	linear	linear



$V_o = V_{DD} - I_{RD} \cdot R_D = V_{DS2} + V_{DS1}$

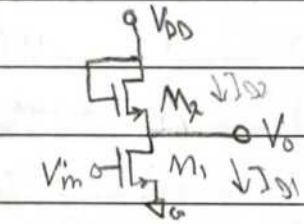
$\therefore I_{D1} = k_{n1} V_{DS1}[2(V_{GS1} - V_{T1}) - V_{DS1}]$ $\wedge$ $I_{RD} = \frac{V_{DD} - V_o}{R_D} = I_{D1} = I_{D2}$

$\wedge I_{D2} = k_{n2} V_{DS2}[2(V_{GS2} - V_{T2}) - V_{DS2}]$

if $V_{GS1} = A$ $\wedge$ $V_{GS2} = B - V_{DS1}$

$\rightarrow \frac{V_{DD} - (V_{DS1} + V_{DS2})}{R_D} = k_{n1} V_{DS1}[2(A - V_{T1}) - V_{DS1}]$
$= k_{n2} V_{DS2}[2(B - V_{DS1} - V_{T2}) - V_{DS2}]$

* NMOS inverter with active load



$\therefore V_{DS2} = V_{GS2} \rightarrow V_{GS2} - V_T < V_{DS2}$

$\rightarrow M_2$ is always saturated regardless of M_1

* Cases:

1- $V_{in} < V_T \rightarrow M_1$ is off $\wedge$ I_{D1} is zero;

$I_{D1} = I_{D2} = 0 \rightarrow k_{n2}(V_{GS2} - V_{TN2})^2 = 0 \rightarrow V_{GS2} = V_{TN2}$

$\therefore V_o = V_{DD} - V_{GS2} = V_{DD} - V_{TN2}$

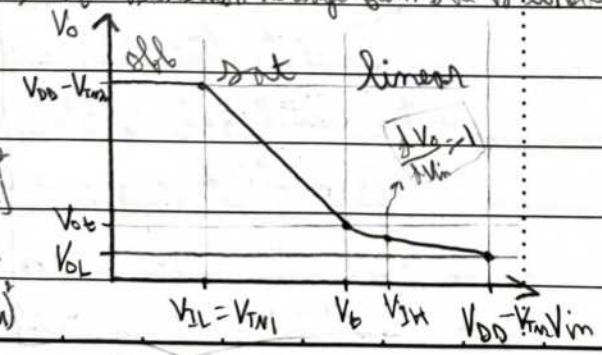
2- $V_{TN1} < V_{in} < V_t \rightarrow M_1$ is sat, V_t: transition voltage from sat to linear

$I_{D1} = k_{n1}(V_{GS1} - V_{TN1})^2 = k_{n1}(V_{in} - V_{TN1})^2$

$V_{GS2} = V_{DD} - V_{DS1} = V_{DD} - V_o$

$I_{D2} = k_{n2}[V_{GS2} - V_{TN2}]^2 = k_{n2}[V_{DD} - V_o - V_{TN2}]$

$\therefore I_{D1} = I_{D2} \rightarrow k_{n2}(V_{DD} - V_o - V_{TN2})^2 = k_{n1}(V_{in} - V_{TN1})$



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$\therefore V_o = V_{DD} - V_{TN2} - \sqrt{\frac{k_{n1}}{k_{n2}}}\cdot(V_{in} - V_{TN}) \rightarrow V_{T1} = V_{TN1}$

3- $V_{in} = V_t \rightarrow M_1$ saturated lohmic (edge)

$V_{DS1} = V_{GS1} - V_{TN1} \rightarrow V_{ot} = V_t - V_{T1} \wedge I_{D1} = I_{D2}$

$k_{n1}(V_{GS1} - V_{TN})^2 = k_{n2}(V_{GS2} - V_{TN2})^2$

$\rightarrow k_{n1}(V_t - V_{T1})^2 = k_{n2}(V_{DD} - V_{ot} - V_{T2})^2 = k_{n2}(V_{DD} - V_t + V_{T1} - V_{T2})^2$

4- $V_{in} > V_t \rightarrow M$ is ohmic:

$I_{D1} = k_{n1} V_{DS1}\left[2(V_{GS1} - V_{T1}) - V_{DS1}\right]$, $V_o = V_{DS1}$, $V_{GS1} = V_{in}$

$\wedge V_{GS2} = V_{DD} - V_o$

$\because I_{D1} = I_{D2} \wedge I_{D2} = k_{n2}(V_{GS2} - V_{T2})^2$

$\rightarrow k_{n1} V_{DS1}\left[2(V_{GS1} - V_{T1}) - V_{DS1}\right] = k_{n2}(V_{GS2} - V_{T2})^2$

- in this region, V_{TH} can be found by taking the derivative of the above equation: $\frac{dV_o}{dV_{in}} = -1$

- taking the second case and solving for V_t:

$$V_t = \frac{\sqrt{\frac{k_{n1}}{k_{n2}}}\cdot V_T + V_{DD}}{1 + \sqrt{k_{n1}/k_{n2}}}$$, define $k_R = \frac{k_{n1}}{k_{n2}}$

$$\rightarrow V_t = \frac{\sqrt{k_R}\cdot V_T + V_{DD}}{1 + \sqrt{k_R}}$$, k_R should be large

$\because k_{n1} = \frac{W_1}{L_1}\frac{\mu_n C_{ox}}{2} \wedge k_{n2} = \frac{W_2}{L_2}\frac{\mu_n C_{ox}}{2}$, $\frac{\mu_n C_{ox}}{2}$ is usually constant

$\therefore k_R = \left(\frac{W_1/L_1}{W_2/L_2}\right)$, ratio of the aspect ratios of the transistors

$\rightarrow M_1$ should be wide and M_2 narrow

example: $V_T = 1V$, $k_{n1} = 10^{-3}\ A/V^2$, $k_{n2} = 0.34\times10^{-3}\ A/V^2$, $V_{DD} = 5V$

1) $V_t = \frac{\sqrt{k_R}\cdot V_T + V_{DD}}{1 + \sqrt{k_R}} \wedge \sqrt{k_R} = 1.715 \rightarrow V_t = 2.493V$

$V_{ot} = V_t - V_T = 1.493V$

2) for $V_{in} = V_{DD} - V_T = 4V$, ohmic $\rightarrow V_o[2(3) - V_o] = \frac{k_{n2}}{k_{n1}}(5 - V_o - 1)^2$

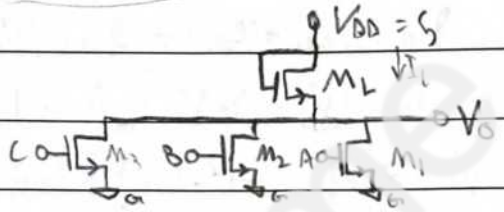
$\rightarrow \frac{k_{n1} + k_{n2}}{k_{n1}}V_o^2 - \frac{6k_{n1} + 8k_{n2}}{k_{n1}}\cdot V_o + \frac{k_{n2}}{k_{n1}}16 = 0$

$\rightarrow \boxed{V_o = 0.6989\ V}$ or 5.8085 out of range

- note on previous example: maximum output voltage of the circuit is $V_{DD} - V_T$, hence the high input corresponding to V_{OL} is $V_{in} = V_{DD} - V_T$

* NMOS NOR gate:

A	B	C	V_{out}	
0	0	0	1	$V_{DD} - V_T$
0	0	1	0	
0	1	0	0	
↓	↓	↓	↓	
1	1	1	0	



$\therefore I_D = k_{n1} V_{DS1} [2(V_{GS1} - V_{T1}) - V_{DS1}]$

$I_L = k_L (V_{GSL} - V_{TL})^2$, $I_L = m I_{D1}$

$\therefore k_L (V_{GSL} - V_T)^2 = m k_{n1} V_{DS1} [2(V_{GS1} - V_T) - V_{DS1}]$

- Worst case when $m = 1$ (one transistor), hence $V_{OL} < V_T$ always

example: $V_T = 1V$, $k_{n1} = 10^{-3}\ A/V^2$, $k_L = 0.34 \times 10^{-3}\ A/V^2$

$\rightarrow k_R = \frac{10^{-3}}{0.34 \cdot 10^{-3}} = 2.94$

1) V_{OL} if $A = B = 1 = 4V$

$k_L (V_{GS1} - V_{T1})^2 = 3 \cdot k_{n1} \cdot V_{OL} [2(4-1) - V_{OL}]$

$\rightarrow (5 - V_{OL} - 1)^2 = 3 \cdot 2.94 \cdot V_{OL} [6 - V_{OL}]$

$\rightarrow 16 - 8V_{OL} + V_{OL}^2 = 8.82 \cdot [6V_{OL} - V_{OL}^2]$

$\rightarrow 9.82 \cdot V_{OL}^2 - 60.92 V_{OL} + 16 = 0 \rightarrow V_{OL} = 0.295\ V$

2) $m = 1 \rightarrow 16 - 8V_{OL} + V_{OL}^2 = 2.94 [6V_{OL} - V_{OL}^2]$

$\rightarrow 3.94 V_{OL}^2 - 25.64 V_{OL} + 16 = 0 \rightarrow V_{OL} = 0.699\ V$

- hence, one active gate gives the highest output voltage

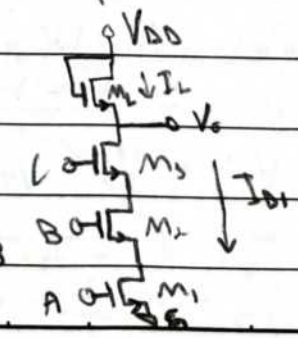
* NMOS NAND gate:

- if any input is low then $V_o = V_{DD} - V_T$
- if all inputs high then output: low logic

all transistors will be ohmic, $V_o = V_{DS1} + V_{DS2} + V_{DS3}$

$V_{GS1} = A = V_{DD} - V_T$, $V_{GS2} = V_{DD} - V_T - V_{DS1}$

$V_{GS3} = V_{DD} - V_T - V_{DS1} - V_{DS2}$



example: $k_1 = k_{n_2} = k_3 = k_n = 2\times10^{-3}\ A/V^2$, $V_{T1} = V_{T2} = V_{T3} = 1V$

λ $I_D = 1mA$, $V_{DD} = 5V$

1) $V_{OL} = V_{DS3} + V_{DS2} + V_{DS1}$

$\because$ $V_{GS1} = 5 - 1 = 4V$

ohmic $\rightarrow$ $I_D = k_n \cdot V_{DS1}[2(V_{GS1} - V_T) - V_{DS1}] = 1mA$

$\Rightarrow 0.5 = 6V_{DS1} - V_{DS1}^2 \rightarrow V_{DS1} = 84.52\ mV$

$\because$ $V_B = V_{DD} - V_T \rightarrow V_{GS2} = V_B - V_{DS1} = 3.9155V$

λ $I_D = k_n V_{DS2}[2(V_{GS2} - V_T) - V_{DS2}] \rightarrow -V_{DS2}^2 + 5.831 V_{DS2} - 0.5 = 0$

$\Rightarrow V_{DS2} = 89.054\ mV$

$\because$ $V_C = V_{DD} - V_T \rightarrow V_{GS3} = V_C - V_{DS1} - V_{DS2} = 3.8284V$

$\rightarrow -V_{DS3}^2 + 5.65686 V_{DS3} - 0.5 = 0 \Rightarrow V_{DS3} = 89.81\ mV$

$\therefore$ $V_{OL} = 89.81 + 89.05 + 84.52 = \boxed{0.2614\ V}$

2) $\because$ load always saturated: $I_D = k_L(V_{GSL} - V_T)^2$

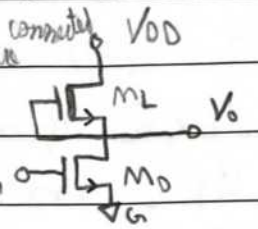
$V_{GSL} = V_{DD} - V_T - V_{OL} = 3.739V \Rightarrow k_L = 71.55\mu A/V^2$

Subject D-NMOS load Date 8/5/2021 No.

$V_{GSL} = 0 \rightarrow M_L$ is always on, since gate and source are connected

$V_{DSL} < V_{GSL} - V_{TL} \rightarrow M_L$ is linear

$V_{DSL} > V_{GSL} - V_{TL} \rightarrow M_L$ is saturated



- since the depletion NMOS has a negative threshold voltage, the device is normally on

① $V_{in} < V_{TD}$, M_D is off, $I_D = 0$:

- M_L could be sat or ohmic.

assuming sat:

$I_D = k_L (0 - V_T)^2 \neq 0$

hence not sat $\rightarrow$ linear

$\therefore I_D = k_L V_{DSL} [2(V_{GSL} - V_T) - V_{DSL}] = 0$

$\rightarrow \boxed{V_{DSL} = 0}$ or $V_{DSL} = 2V_{TL}$, which is larger than $V_{GSL} - V_{TL}$ hence breaks the condition for sat

$\therefore \boxed{V_o = V_{DD}}$

② $V_{in} > V_{TD}$, M_D becomes saturated, M_L remains linear:

$k_1 (V_{GS1} - V_{TD})^2 = k_L V_{DSL} [2(V_{GSL} - V_{TL}) - V_{DSL}]$

$\therefore k_1 (V_i - V_{TD})^2 = k_L (V_{DD} - V_o) [-2V_{TL} - (V_{DD} - V_o)]$

then find V_{IL}

③ at $V_{in} = V_{SS}$, M_D will stay in sat, whereas M_D will enter sat:

FOS: $V_{DS1} = V_{GS1} - V_{T1} = V_{SS} - V_{T1} = V_{OSS}$

& $k_1 (V_{GS1} - V_{TD})^2 = k_L (V_{GSL} - V_{TL})^2$ & $V_{GSL} = 0$ & $V_{GS1} = V_{SS}$

$\therefore V_{SS} = V_{TD} \pm \sqrt{\frac{k_L}{k_1}} \cdot V_{TL}$

$\rightarrow \boxed{V_{OSS}^2 = \frac{k_L}{k_1} \cdot V_{TL}^2}$

	①	②	③	④
M_L	linear	linear	sat	sat
M_D	cutoff	linear	sat	linear

④ $V_{in} > V_{SS}$, M_D is linear, M_L remains saturated

$k_1 V_{DS1}[2(V_{GS1} - V_{T1}) - V_{DS1}] = k_L (V_{GSL} - V_{TL})^2$

$\rightarrow k_1 V_o [2(V_i - V_{T1}) - V_o] = k_L (0 - V_{TL})^2$

then find V_{TH} or V_{OL} if $V_i = V_{DD}$

- V_{OL} is the output voltage corresponding to an input equal to V_{DD}
- larger $\frac{k_1}{k_L}$ makes the curve steeper and closer to ideal

example: $V_{T1} = 1V$, $V_{TL} = -1V$, $k_1 = 1 \times 10^{-3}\ A/V^2$

$k_L = 0.2 \times 10^{-3}\ A/V^2$, $V_{DD} = 5V$. find V_{SS}, V_{OSS}, and V_{OL}

$\therefore V_{SS} = V_{T1} \pm \sqrt{\frac{k_L}{k_1}} \cdot V_{TL} \rightarrow V_{SS} = 0.553V$ or $1.447V$

$0.553 \rightarrow V_{GSL} = V_{in} - V_{T1} \rightarrow$ negative $\rightarrow M_1$ cutoff ✗

$\therefore V_{SS} = 1.447\ V$

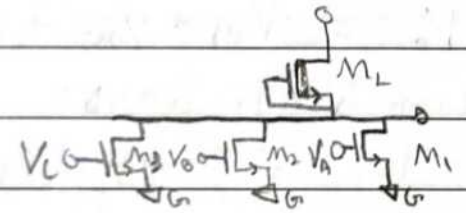
$\therefore V_{OSS} = \pm V_{TL}\sqrt{\frac{k_L}{k_1}} \rightarrow V_{OSS} = 0.447V$

for V_{OL} ④ $\rightarrow k_1 V_o [2(V_{DD} - V_{T1}) - V_o] = k_L (-V_{TL})^2$

$\therefore 2V_o(4) - V_o^2 = 0.2 \rightarrow V_o = 25\ mV$

* N-MOS NOR gate:

A	B	C	V_o
0	0	0	V_{DD}
0	0	1	V_{OS1}
↓	↓	↓	↓
1	1	1	V_{OS1}



load is set and others active $\rightarrow I_L = k_L (V_{GSL} - V_{TL})^2$

$\therefore I_L = m I_D$, m: number of transistors for input

$M_1 \rightarrow 3$ are linear: $I_D = k_D \cdot V_{DSD}[2(V_{GSD} - V_{TD}) - V_{DSD}]$

$\therefore m I_D = m k_D \cdot V_{DSD}[2(V_{GSD} - V_{TD}) - V_{DSD}] = k_L (V_{GSL} - V_{TL})^2$

- worst case is when $m=1$ $\wedge$ $V_{OL} < V_{T1}$

example on NMOS NOR

① $A=B=C=5V \rightarrow m=3$

$\rightarrow 3 \cdot k^{-3} \cdot V_o[2(V_{DD}-V_{T1})-V_o] = 0.34\times10^{-3}(-V_{TL})^2$

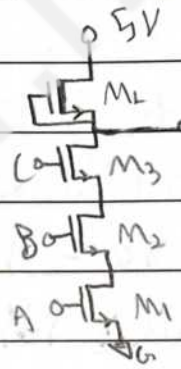
$\rightarrow 8V_o - V_o^2 = \frac{17}{150} \rightarrow V_o = 14.14\ mV$

② if $A=5$ & $B=C=0V \rightarrow m=1$

$\therefore 8V_o - V_o^2 = 0.34 \rightarrow V_o = 42.93\ mV$

* NMOS NAND gate:

- any low input gives $I_L=0$ & $V_o=V_{DD}$
- if all inputs are high ($A=B=C=V_{DD}$), then all MOSFETs are in linear mode



$\rightarrow V_{GS1} = A = V_{DD}$

$V_{GS2} = B - V_{DS1} = V_{DD} - V_{DS1}$

$V_{GS3} = V_{DD} - V_{DS1} - V_{DS2}$

$V_o = V_{DS1} + V_{DS2} + V_{DS3}$

example on NMOS NAND:

① $V_{o1} = V_{DS1} + V_{DS2} + V_{DS3}$ & $I_D = 1mA = k_{n1}(-V_{Tn})^2$

$= k_{nD} \cdot V_{DSx}(2(V_{GSx}-V_{Tn})^2 - V_{DSx})$

$\therefore -V_{DSx}^2 + 2(V_{GSx}-1)\cdot V_{DSx} - 0.5 = 0$

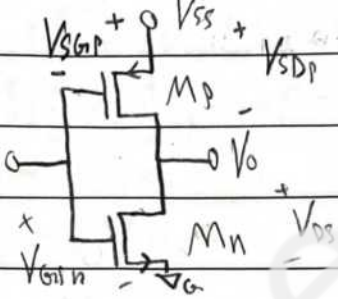
$\rightarrow V_{DS1} = 62.99\ mV$, $V_{DS2} = 64.02\ mV$, $V_{DS3} = 65.09\ mV$

$\therefore V_{o1} = 0.1921\ V$

② $\because 1mA = k_{nL}$

Subject CMOS logic Date 8/6/2021 No.

* CMOS: complementary metal oxide semiconductors
* CMOS inverter: consists of NMOS and PMOS



① $0 < V_{in} < V_{TN}$, M_n off, M_p ohmic:

$k_p V_{SDp}[2(V_{SGp} - |V_{TP}|) - V_{SDp}] = 0 \rightarrow V_{SDp} = 0$

$\rightarrow V_o = V_{DD}$

② $V_{TN} < V_{in} < V_{SS}$, M_n sat, M_p ohmic:

$\rightarrow k_n (V_{GSn} - V_{TN})^2 = k_p V_{SDp}[2(V_{SGp} - |V_{TP}|) - V_{SDp}]$

$\therefore k_n (V_{in} - V_{TN})^2 = k_p (V_{DD} - V_o)[2(V_{DD} - V_{in} - |V_{TP}|) - (V_{DD} - V_o)]$

③ $V_{in} = V_{SS}$, M_n sat, M_p sat:

$\rightarrow k_n (V_{GSn} - V_{TN})^2 = k_p (|V_{GSp}| - |V_{TP}|)^2$

$\therefore k_n (V_i - V_{TN})^2 = k_p (V_{DD} - V_i - |V_{TP}|)^2$

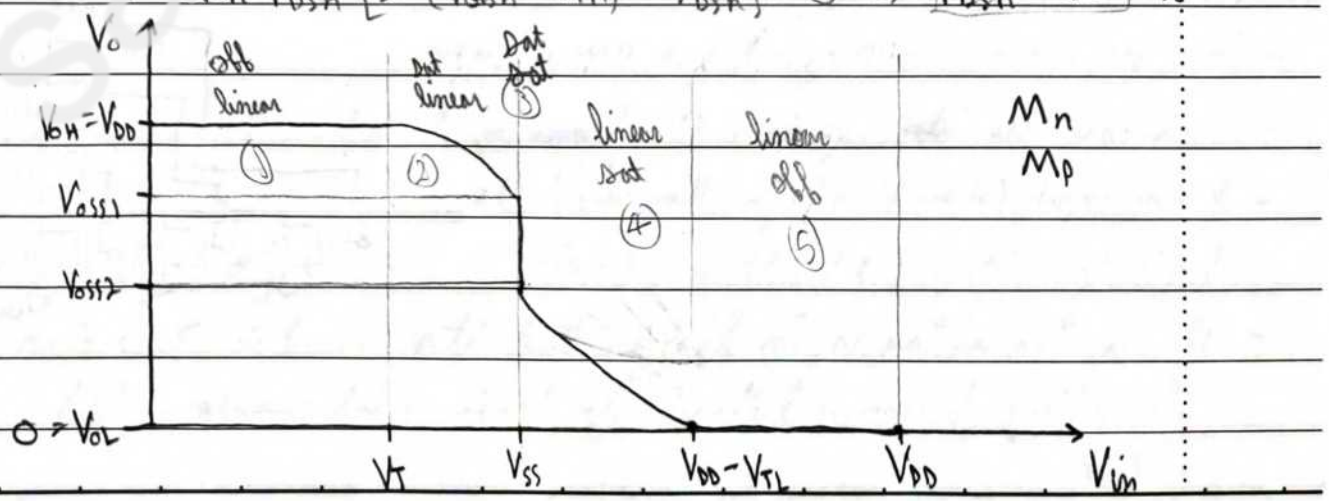
④ $V_{SS} < V_{in} < V_{DD} - V_{TN}$, M_n ohmic and M_p sat:

$k_n V_{DSn}[2(V_{GSn} - V_{TN}) - V_{DSn}] = k_p (V_{GSp} - |V_{TP}|)^2$

$\therefore k_n V_o[2(V_i - V_{TN}) - V_o] = k_p (V_{DD} - V_i - |V_{TP}|)^2$

⑤ $V_{DD} - V_T < V_{in} < V_{DD}$, M_n is ohmic, M_p is off:

$\rightarrow k_n V_{DSn}[2(V_{GSn} - V_{TN}) - V_{DSn}] = 0 \rightarrow V_{DSn} = 0V = V_o$



tips for using PMOS:
- replace V_{GS} with V_{SG} and replace V_{DS} with V_{SD} in order to use NMOS equations
- use $|V_{TP}|$ for the threshold

MODE: $V_{SGp} > |V_{TP}| \rightarrow$ on
$V_{SDp} > V_{SGp} - |V_{TP}| \rightarrow$ sat

* advantages of CMOS logic:

- low power dissipation - better packaging design - high noise immunity

- if $I_{Dn} = I_{Dp}$, $k_n(V_{GSn} - V_{Tn})^2 = k_p(V_{SGp} - |V_{Tp}|)^2$

$$\rightarrow V_{SS} = \frac{V_{Tn} + \sqrt{\frac{k_p}{k_n}}\left[V_{DD} - |V_{Tp}|\right]}{1 + \sqrt{\frac{k_p}{k_n}}}$$

if $k_n = k_p$ & $V_{Tn} = |V_{Tp}|$

$$\rightarrow V_{SS} = \frac{V_{DD}}{2}$$

- at V_{SS}, M_n switches from sat to linear:

EOS $\rightarrow V_{DSn} = V_{GSn} - V_{Tn} = V_{SS} - V_{Tn} = V_{OSS1}$

- at V_{SS}, M_p switches from linear to sat

$\rightarrow V_{SDp} = V_{SGp} - |V_{Tp}| = V_{DD} - V_{SS} - |V_{Tp}|$

& $V_{SDp} = V_{DD} - V_o \rightarrow V_{DD} - V_{SS} - |V_{Tp}| = V_{DD} - V_o$

$\therefore V_o = V_{SS} + |V_{Tp}| = V_{OSS2}$

example on inverter:

① if $k_n = k_p$ & $V_{Tn} = |V_{Tp}| \rightarrow V_{SS} = \frac{V_{DD}}{2} = 2.5V$

② if $V_{in} = V_{SS} \rightarrow$ both sat

$I_p = k_p(V_{SGp} - |V_{Tp}|)^2$ & $V_{SG} = V_{DD} - V_{in}$

$\rightarrow I_p = k_p(2.5 - 1)^2 \rightarrow I_p = 4.5\,mA$

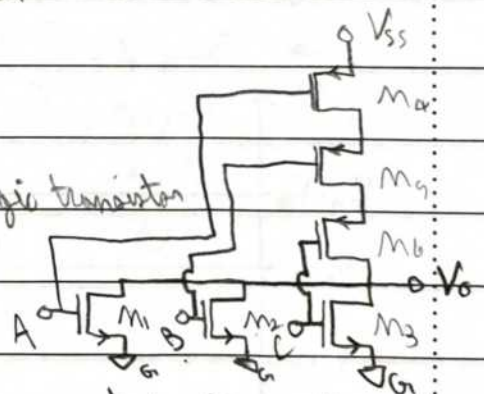
* NOR CMOS:

- two transistors are required for every input

- every input transistor requires a complementary logic transistor

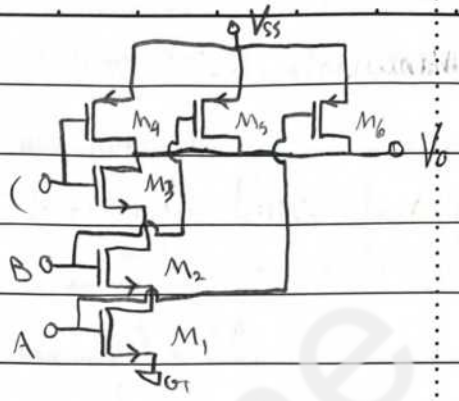
- if one input (at least) is high, then one of the logic transistors (at least) will be off

- if a transistor is in linear but its current is zero then the voltage difference between its drain and source will be zero



NAND CMOS:

- If one of the input transistors has slow voltage, it will be cutoff, causing the other transistors' currents to equal zero hence the output voltage will be high.



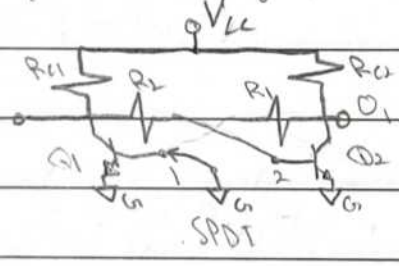
Subject Chapter 8: Timing circuits Date 8/5/2024 No.

* multivibrators: sequential logic circuits that operate continuously between two distinct states of high and low

+ Types of multivibrators:

- Astable: free-running multivibrator that has no stable states but switches continuously between two states, producing a train of square-wave pulses at a fixed frequency
- monostable: a one-shot multivibrator that has only one stable state and is triggered externally and returns back to its first, stable, state
- bistable: a flip-flop that has two stable states, which produces a single pulse (either positive or negative)

* bistable multivibrators:



- When SPDT is at position [1], Q_1 will be cutoff and output O_1 will go high. Q_2 will in turn go to sat and O_2 will be low
- This state will remain unless the switch is flipped (externally)

$$\rightarrow I_{B1} = I_{B2} = \frac{V_{CC} - V_{BE2\,sat}}{R_{C1} + R_2}$$

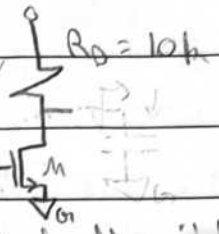
$\therefore V_{O1} = V_{CC} - I_{B1} \cdot R_{C1}$ & $V_{O2} = V_{CE2\,sat} = 0.1V$

- If the switch connects to position [2], Q_2 will cutoff O_2 will be high, and soon.
- linear and reverse active modes are ignored in multivibrators

Subject Capacitive effects of MOSFETs Date 10/5/2021 No.

given $C_L = 50\ fF = 50 \times 10^{-15}\ F$, $V_{OL} = 0.6V$, $V_{OH} = 5V$

$V_T = 1$ & $k_n = 100\ \mu A/V^2$



- If the input is low, output should switch to high

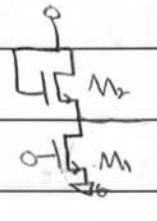
$\therefore i = C\frac{dV_o}{dt} = \frac{V_{DD} - V_o}{R_D}$

- If the input switches from low to high, output should switch back to low : $I_D = I_{RD} + I_{Co}$, $I_{Co} = -\frac{dV_o}{dt} \cdot C$

if $V_o > 4$: M → sat → $I_D = k_n[V_{GS} - V_{TN}]^2 = \frac{V_{DD} - V_o}{R_D} - C\frac{dV_o}{dt}$

if $V_o < 4$: M → ohmic → $I_D = k_n \cdot R_D[8V_o - V_o^2] = \frac{V_{DD} - V_o}{R_D} - C\frac{dV_o}{dt}$

* NMOS with saturated ENMOS as load:



input going from high to low:

$\therefore M_2$ sat → $I_{D2} = k_{n2}(V_{DD} - V_o - V_{T2})^2$

$\therefore i_L = C\frac{dV_o}{dt} = k_{n2}(4 - V_o)^2$

* NMOS inverter with DNMOS as load : $V_{GS1} = 0$

$V_{TL} = -2V$ $V_{TD} = 1V$

$k_L = 25\ \mu A/V^2$

$V_{OL} = 0.1V$

$V_{OH} = 5$ $k_D = 75\ \mu A/V^2$

for $V_o < 3$: $V_{DSL} > V_{GSL} - V_{TL}$ → Sat

$\therefore I_D = C\frac{dV_o}{dt} = k_L(V_{GSL} - V_{TL})^2$

$= k_L(-V_{TL})^2$

$\therefore \boxed{V_o(t) = V_{OL} + \frac{k_L}{C}(V_{TL})^2 t}$

for high to low input

for $V_o > 3$: $V_{DSL} < -V_{TL}$ → ohmic

$I_D = C\frac{dV_o}{dt} = k_L R_D(2(V_{GSL} - V_{TL}) \cdot V_{DSL} - V_{DSL}^2)$

$\rightarrow C\frac{dV_o}{dt} = k_L \cdot R_D(4(V_{DD} - V_o) - (V_{DD} - V_o)^2)$

- NMOS with DNMOS load as input goes from low to high

if $V_o > 4$: M_L ohmic, M_D sat $\because V_{DSD} > V_{GSD} - V_{TD}$

$\rightarrow I_D = k_D \cdot (V_{GSD} - V_{TD})^2 = 1.2mA$

if $V_o > 3$ → M_L : $I_D = k_L(4(V_{DD} - V_o) - (V_{DD} - V_o)^2)$

Subject Date No.

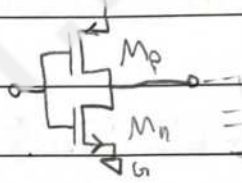
* for $3 < V_o < 4$, M_D & M_L ohmic

M_D: $I_D = k_{nD}(8V_o - V_o^2) = k_L(4(V_{DD}-V_o) - (V_{DD}-V_o)^2)$

* for $V_o < 3$, M_L is sat & M_D is linear

- hence, an ENMOS driver connected to a DNMOS load will pass through three stages (M_L linear & M_D sat, both linear, and M_L sat & M_D linear) while switching from low input to high input (or high output to low)

* CMOS inverter:



• high to low input:

M_p sat initially: $I_D = k_p(V_{DD} - V_i - |V_{TP}|)^2$

for $V_o < |V_{TP}|$ $= k_p(V_{DD} - |V_{TP}|)^2 = C\frac{dV_o}{dt}$

$\therefore V_{SS} - V_o > V_{SS} - V_i - |V_{TP}|$ $(V_{SD} > V_{SG} - V_{TP})$ condition for sat

- if $V_o > |V_{TP}|$ → M_p goes to ohmic mode

→ $C \cdot \frac{dV_o}{dt} = k_p(2(V_{DD} - |V_{TP}|)(V_{DD} - V_o) - (V_{DD} - V_o)^2)$

• for low to high input:

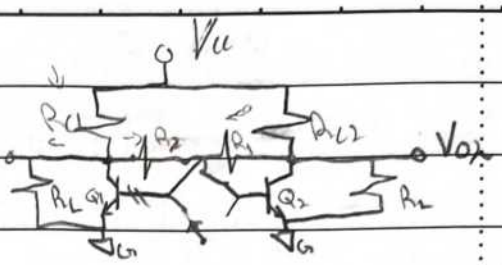
- initially M_n will be sat, M_p will be cutoff

→ $C\frac{dV_o}{dt} = -k_n(V_{DD} - V_{TN})^2$

- next the driver will enter linear, whereas M_p will remain off:

$$C\frac{dV_o}{dt} = -k_n(2(V_{DD} - V_{TN})V_o - V_o^2)$$

* loaded bistable MV:



- Q_1 is off since its base is grounded V_{o1}
- Q_2 is saturated

$$I_{L2} = \frac{V_{CE2\,sat}}{R_L} = \frac{0.1}{R_L}$$

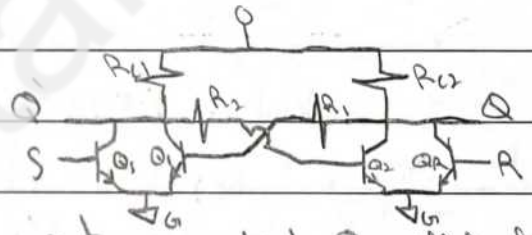
$$I_{L1} = I_{RC1} - I_{B2} \rightarrow \frac{V_{o1} - V_{CE2\,sat}}{R_2} = \frac{V_{cc} - V_{o1}}{R_{L1}} - \frac{V_{o1}}{R_L}$$

- for Q_2 to be saturated, $I_{C2} \geq \beta_2 \cdot I_{B2}$

$$I_{C2} = \frac{V_{cc} - V_{o2}}{R_{L2}} - \frac{V_{o2}}{R_L}$$

$$\therefore \beta_2 \left[\frac{V_{cc} - V_{o1}}{R_{L1}} - \frac{V_{o1}}{R_2} \right] \leq \left[\frac{V_{cc} - 0.1}{R_2} - \frac{0.1}{R_L} \right]$$

* RS flip-flop using bistable:



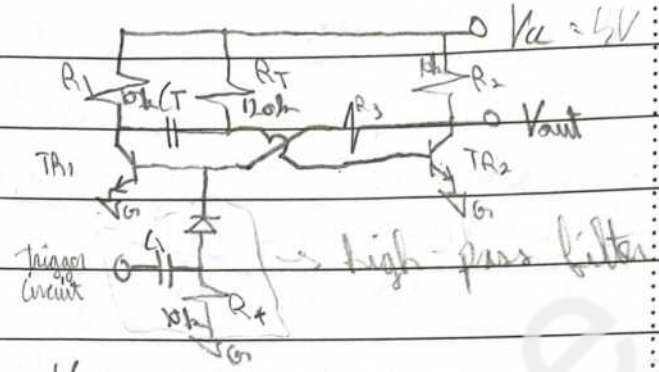
- If the S input is low while the R input is high Q_1 will be off, Q_2 will be sat → output Q will be low ∴ Q output is low and connected to the base of Q_1, then the output $\bar{Q}$ will be high since Q_1 will be off

R	S	Q	
0	0	Q(t-1)	holds previous
0	1	1	set
1	0	0	reset
1	1	X	indeterminate

Q_1 off, Q_2 sat
Q_1 off, Q_2 off
Q_1 sat, Q_2 off
Q_1 off, Q_2 sat

Subject Monostable and Astable MVs Date 12/5/2024 No.

* monostable multivibrator:



- before Triggering, TR_2 will be saturated, giving TR_1 off.
the voltage difference across $C_T = 5 - 0.8$
$V_{CC} - V_{BE(sat)2}$, $V_{out} = 0.1V$
- the voltage on both terminals of the capacitor must drop by the same amount, hence C_T after the trigger: $0.1 \xrightarrow{C_T} -0.8 - (V_{CC} - 0.1)$
since TR_1 is saturated as $V_{BE1} = 0.8V$, TR_2 goes off
∴ during trigger: $V_{out} = V_{CC} - I_{R2} \cdot R_2$, $I_{R2} = \frac{V_{CC} - V_{BE(sat)}}{R_2 + R_3}$
$\rightarrow \frac{5 - 0.8}{20k} = 0.2mA \rightarrow V_{out} = 2.6V$
otherwise, $V_{out} = V_{CE2sat} = 0.1V$
C_T charging: $V_{B2}(t) = V_{B2}(\infty) - [V_{B2}(\infty) - V_{B2}(0)]e^{-t/\tau}$
$V_{B2}(\infty) = V_{CC}$, $V_{B2}(0) = 0.8 - (V_{CC} - 0.1)$
$\therefore V_{B2}(t) = V_{CC} - [2V_{CC} - 0.9]e^{-t/\tau}$
$= 5 - 9.1e^{-t/\tau}$, $\tau = R_T \cdot C_T$
- to find the pulse duration, set $V_{BE}(t) = V_{B2}(T)$ equal to the stable value of $V_{BE(sat)} = 0.8$
$\therefore V_{B2}(T) = 0.8 = 5 - 9.1e^{-T/\tau} = V_{CC} - [2V_{CC} - 0.9]e^{-t/\tau}$
$\rightarrow e^{-T/\tau} = \frac{V_{CC} - 0.8}{2V_{CC} - 0.9} \approx \frac{1}{2}$ assuming $V_{CC} \gg 1$
$\rightarrow T = \tau \cdot \ln(2) = R_T \cdot C_T \cdot \ln(2)$
- monostable circuits are called "one-shot" as they give a high output pulse which returns to the stable steady-state low output
- the duration between pulses from the triggering circuit should be $5 \cdot R_1 \cdot C_T$

Subject quiz 2&3 practice Date 17/5/2021 No.

NMOS:

$V_{GS} < V_{TN}$ — off

$V_{GS} > V_{TN}$

$V_{DS} > V_{GS} - V_{TN}$ | $V_{DS} < V_{GS} - V_{TN}$

sat: $I_D = k_n (V_{GS} - V_{TN})^2$ ohmic: $I_D = k_n [2(V_{GS} - V_{TN}) V_{DS} - V_{DS}^2]$

example:

a) $V_{in} = V_{GS} = 3V \Rightarrow V_o = 0.1V$

$V_o = V_{DS}$ on if $V_o = 0.1 \Rightarrow V_{DS} < V_{GS} - V_{TN}$

$\Rightarrow$ ohmic $\therefore I_D = k_n [2(V_{GS} - V_{TN}) V_{DS} - V_{DS}^2]$

$I_D = \frac{3 - 0.1}{R_D}$

$\Rightarrow \frac{2.9}{R_D} = 150\mu [2(2.5)0.1 - (0.1)^2]$

$\Rightarrow R_D = 39.46\ k\Omega$

b) substituting in equation

$$V_S = V_{TN} - \frac{1}{2R_D k_n} \pm \sqrt{\left(\frac{1}{2R_D k_n}\right)^2 + \frac{V_{DD}}{R_D k_n}}$$

$\Rightarrow V_S = 0.5 - 0.08449 \pm 0.7190148$

$\Rightarrow V_S = 1.13252$

example: $V_t \Rightarrow$ transition point from sat to linear

N_1 sat $\wedge$ load N_2 linear

1) $k_{n1}(V_{GS1} - V_{TN1})^2 = k_{n2}[2(V_{GS2} - V_{TN2}) V_{DS2} - V_{DS2}^2]$

$\frac{k_{n1}}{k_{n2}} = \frac{1}{0.34}$ $\wedge$ $V_{GS1} = V_{in} = V_t \wedge V_{T1} = V_{T2} = V_T$

$\Rightarrow \frac{1}{0.34}(V_t - 1)^2 = 2(V_{DD} - V_o - 1)(V_{DD} - V_o) - (V_{DD} - V_o)^2$

$V_o = V_{ot} = V_t - V_{TN} \Rightarrow \frac{1}{0.34}(V_t - 1)^2 = 2(6 - V_t)(6 - V_t) - (6 - V_t)^2$

$\Rightarrow \frac{1}{0.34}[V_t^2 - 2V_t + 1] = 2[36 - 12V_t + V_t^2] - (36 - 12V_t + V_t^2)$

$\Rightarrow \frac{1 - 0.34}{0.34} V_t^2 - \frac{2 + 3.4}{0.34} V_t - 21.0588 = 0$

$\Rightarrow V_t = 2.39965$ or ~~-4.2~~ $\Rightarrow V_{ot} = 1.39965$

1) load is always sat: $V_{ot} = V_t - V_T$

$k_{n1}(V_t - V_T)^2 = k_{n2}(V_{DD} - V_o - V_T)^2$

$k_{n1}/k_{n2} = 1/0.34 \rightarrow V_t^2 - 2V_t + 1 = 0.34(5^2 - 10V_t + V_t^2)$

$\rightarrow V_t = 2.49330$ ∧ $V_{ot} = 1.49330$

2) $V_{in} = 5 - 1 = 4V$

M_1 is ohmic $V_{GS1} = 4$

$\rightarrow k_{n2}[V_{DD} - V_o - 1]^2 = k_{n1}[2(V_{GS1} - V_T)V_{DS1} - V_{DS1}^2]$

$\rightarrow 0.34[4 - V_o]^2 = 6V_o - V_o^2$ $V_o = V_{DS1}$

$\rightarrow 0.34[16 - 8V_o + V_o^2] = 6V_o - V_o^2 \rightarrow V_o = 0.69892$

example:

1) $k_n(V_{GSL} - V_{TL})^2 = m k_{n1}[2(V_{GS1} - V_{T1})V_{DS1} - V_{DS1}]$

$\rightarrow 0.34(5 - V_o - 1)^2 = 3 \cdot [2V_o(3) - V_o^2]$

$\rightarrow 0.34(4 - V_o)^2 = 18V_o - 3V_o^2$

$\rightarrow V_{oL} = 0.274913$

2) $0.34[16 - 8V_o + V_o^2] = 6V_o - V_o^2$

$\rightarrow V_{oL} = 0.6989$

example: V_{oL} → all inputs high. $I_D = 1mA$. all ohmic

→ M_1: 0 / input high = high output = $V_{DD} - V_{TL}$

$1mA = 2\times10^{-3}[2(V_{DD} - V_{TL} - V_{T1})V_{DS1} - V_{DS1}^2]$

$\rightarrow 0.5 = 2(3)V_{DS1} - V_{DS1}^2$

$\rightarrow V_{DS1} = 0.084524$

M_2: $1mA = 2\times10^{-3}[2(V_{DD} - V_{TL} - V_{DS1} - V_{T2})V_{DS2} - V_{DS2}^2]$

$\rightarrow 0.5 = 5.830952 V_{DS2} - V_{DS2}^2$

$\rightarrow V_{DS2} = 0.089048852$

M_3: $V_{GS3} = V_{DD} - V_{TL} - V_{DS1} - V_{DS2} = 3.5284 2918$

$\therefore 0.5 = 6.656854 V_{DS3} - V_{DS3}^2$

$\rightarrow V_{DS3} = 0.0898143$

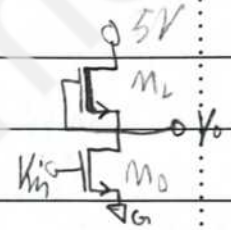
$\rightarrow V_{OL} = V_{DS1} + V_{DS2} + V_{DS3} = \underline{0.261387\,V}$

$\therefore I_D = k_{n1}[V_{GS1} - V_{TL}]^2$

$V_{GS1} = V_{DD} - V_{OL}$

$\rightarrow \frac{1m}{k_{n1}} = [4.738613 - 1]^2 \rightarrow k_{n1} = 71.545\ \mu A/V^2$

example:



$V_{SS} = V_{TI} \pm \sqrt{\frac{k_{nL}}{k_{n1}}}\, V_{TL}$

$= 1 \pm \sqrt{0.2 \cdot (-1)} = 0.552786$ or $1.447214\,V$

$\rightarrow V_{SS} = 1.447214\,V$

$\wedge\ V_{OSS}^2 = \frac{k_{nL}}{k_{n1}} V_{TL}^2 \Rightarrow V_{OSS} = \pm\sqrt{\frac{k_{nL}}{k_{n1}}} \cdot V_{TL}$

$\rightarrow V_{OSS} = \pm\sqrt{0.2} = 0.447\,2\,V$

to find V_{OL}: M_L is sat $V_{GS} > V_T \wedge V_{DSL} > V_{GS} - V$

$\rightarrow I_{DL} = k_{nL}[V_{GSL} - V_T]^2 = k_{nL}[1]^2$

$\wedge\ I_{DD} = I_{DL} = k_D[2(V_{in} - V_{TD})V_o - V_o^2]$

$\rightarrow 0.2 = 8V_o - V_o^2 \rightarrow V_{OL} = 0.025\,1\,V$

example:

$k_{nL}(V_{GSL} - V_{TL})^2 = m\,k_{nm}[2(V_{GS1} - V_{TN})V_o - V_o^2]$

$\rightarrow 0.34 = m[8V_o - V_o^2]$

(a) $m=3 \rightarrow V_{OL} = 0.014192\,V$

(b) $m=1 \rightarrow V_{OL} = 0.042\,93\,V$

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example: $I_D = 1mA$

a) M_1: $0.5 = 8V_{DS1} - V_{DS1}^2 \rightarrow V_{DS1} = 0.0629V$

M_2: $0.5 = 2(4 - V_{DS1})V_{DS2} - V_{DS2}^2 = 0.0640V$

M_3: $0.5 = 2(4 - V_{DS1} - V_{DS2})V_{DS3} - V_{DS3}^2 = 0.0650V$

$\rightarrow V_{OL} = 0.1921V$

b) $I_D = 1mA = k_L(V_{GSL} - (-1))^2 \rightarrow k_L = 1mA/V^2$

example

a) $k_n = k_p \rightarrow V_{TN} = |V_{TP}| \rightarrow V_{SS} = \frac{V_{DD}}{2}$

$\rightarrow V_{SS} = 2.5V$

b) both sat $\rightarrow I_D = k_p(V_{SG} - |V_{TP}|)^2$

$= k_n(V_{GSn} - V_{TN})^2$

$= 2 \times 10^{-3} \cdot (2.5 - 1)^2 = 4.5mA$

past mid exam practice:

1) $k_R = \frac{k_{n1}}{k_{n2}}$

$I_D = k_{n2}(-(-1.2))^2 =$

$V_{SS} = V_{TI} \pm \sqrt{\frac{k_L}{k_A}} \cdot V_{TL}$

$\rightarrow 1.6 = 1 + 1.2 \cdot \sqrt{\frac{I}{k_A}} \rightarrow 0.25 = \frac{1}{k_A}$

$\rightarrow k_A = 4$

2) $V_{SS} \rightarrow$ both sat

$\rightarrow I_{DD} = I_{DL} \rightarrow k_{n1} \cdot (V_{in} - V_T)^2 = k_{nL}(-V_{TL})^2$

$\rightarrow k_R = \frac{(1.2)^2}{(1.6-1)^2} \rightarrow k_R = 4$

3) $NM_L = V_{IL} - V_{OL}$, $V_{OL} =$

b) $V_{OL} = 0.2$ $V_{IL} = 1.2 \rightarrow NM_L = 1$

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7) $NM_H = V_{OH} - V_{IH}$ $V_{OH} = V_{DD}$

$V_{IH} = V_{TN} \rightarrow NM_H = 4$

$V_{IL} = V_{TN} + \frac{1}{2R_D k_n}$ $\lim_{R_D \to \infty} = V_{TN}$

8) $\because V_I = 4.2\,V \rightarrow$ high

$V_{SG} = 0.8\,V\ (5 - 4.2)$

for on $V_{SG} > |V_{TP}|$ ✗ $\rightarrow$ load is off

$\rightarrow V_{DL} = 0 \rightarrow V_{DSL} = 5$

9) $P_{avg} = \frac{P_{IH} + P_{IL}}{2}$ $\because P_{IL} = 0$

$P_{IH} = \frac{(5-0.5)^2}{1k} = \frac{20.25\,mW}{2} =$

$\frac{1}{2}[VI] = \frac{5}{2} \cdot \frac{4.5}{1k} = 11.25\,mW$

10) $\because V_{in} = 0.3 \rightarrow M_1$ off

$V_o = 5 \rightarrow V_{DS2} = V_{DD} - V_o = 0$

11) $\because V_{in} = 1.2 \rightarrow V_{GS1} - V_{TN} = 0.2$

$V_o \; ? \; 0.2$

M_1: $5 - V_o \; ? \; 1.2$

If $V_o > 0.2 \rightarrow$ linear

If $V_o < 0.2 \rightarrow 5 - V_o > 1.2$ sat

or ✗ ✗

$V_o = 4.6 \rightarrow V_{DS1} = 0.4\,V < V_{GS1} - V_{TN}$

$\rightarrow$ Load is linear

$V_{DS1} = 4.6 \rightarrow 4.6 > V_{GS1} - V_{TN1} \rightarrow$ sat

B) $k_n \cdot (V_{in} - 0.8)^2 = (V_{DD} - V_o - 1.2)^2$

$\rightarrow 1 = 5 - V_{DSD} - 1.2$

$V_{DSD} = 2.8\,V$

C) $V_{GSn} = 1.5 \rightarrow V_{DSn} \geq 0.5$

$V_{SGp} = 3.5$

$V_{SDp} > |V_{SGp} - V_{Tp}|$ for sat

$V_{SDp} = V_{SS} - V_o$

$k_n \neq k_p \rightarrow V_{SS} = \dfrac{V_{Tn} + \sqrt{\frac{k_p}{k_n}}\,[V_{DD} - |V_{Tp}|]}{1 + \sqrt{\frac{k_p}{k_n}}}$

$\rightarrow V_{SS} = \dfrac{1 + 0.5\,[V_{DD} - 1]}{1.5}$

$\rightarrow V_{SS} = \frac{2}{3} + \frac{1}{3} V_{SS} - \frac{1}{3}$

$\rightarrow \frac{2}{3} V_{SS} = \frac{1}{3} \rightarrow V_{SS} = 0.5\,V$

$\therefore$ M_p ohmic

$V_{SS} = \dfrac{V_{Tn} + \sqrt{\frac{k_p}{k_n}}\,[V_{SS} - |V_{Tp}|]}{1 + \sqrt{\frac{k_p}{k_n}}}$

$\rightarrow V_{SS} = \dfrac{1 + 0.5\,[V_{SS} - 1]}{1 + 0.5}$

$\rightarrow 1.5 V_{SS} - 0.5 V_{SS} = 0.5 \rightarrow V_{SS} = 0.5$

V_{SS} saturation $\neq V_{SS}$ ohmic

$\rightarrow 1.5 V_{SS\,sat} - 0.5 V_{SS} = 0.5$

$\therefore V_{SS} = \dfrac{0.5 + 2.5}{1.5} = 2\,V$

$V_{Tn} < V_{in} < V_{SS} \rightarrow M_n$ sat M_p ohmic

$I_D = 200\mu\left[1.5-1\right]^2 = 50\mu A$

Q3) $V_{GSL} = V_{DD} - V_o$

$V_{DSL} = V_{DD} - V_o \Rightarrow V_{DSL} = V_{GSL}$

∵ Sat $\rightarrow V_{DSL} \geq V_{GSL} - 1.2$

$V_o = V_{DD} - V_{GSL} = 5 - 1.2 = V_o$

$V_{DSL} = 5 - V_o = 1.2\,V$

Q5) $I_{DD} = I_{DL} \rightarrow (V_{GSD} - V_{TD})^2 = (V_{GSL} - V_{TL})^2$

$V_{GSL} = 5 - V_o \quad \& \quad V_{GSD} = V_{in} = 2.4$

$\rightarrow 2.4 - 0.8 = 3.8 - V_o \rightarrow V_o = 2.2V$

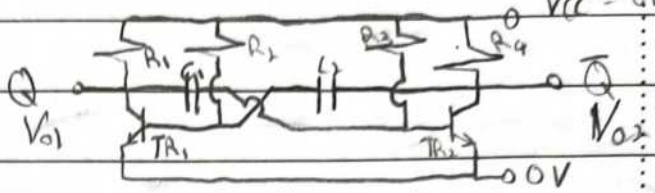
Q8) max power dissipation in CMOS occurs when both transistors are sat

Q9) $V_{DS1} = 1.5 > V_{in} - V_{TN} \rightarrow$ sat M_1

∵ M_2: $V_{DS2} = 0.5 < |-1.2| \rightarrow$ linear

Subject multivibrators (continued) Date 21/5/2021 No.

Astable multivibrators:



1- if TR_1 is off, TR_2 is sat, $V_{o1} = V_{cc}$, $V_{o2} = 0.1$:

V_{cc} — C_1 — 0.8V $0.8 - V_{cc} - R_2 \cdot 0.1$

$C_1 = C_2$ ∧ $R_2 = R_3$

2- C_2 will start charging through R_2 until $V_{B1} = 0.8$ when TR_1 turns to sat and TR_2 turns off → $V_{o1} = 0.1$ V ∧ $V_{B2} = V_{cc}$

0.1 — C_2 — $0.8 - V_{cc} - 0.1$) 0.8 — V_{cc}

3- C_1 will then start to charge through R_3 until $V_{B2} = 0.8$V which is when TR_2 becomes sat and TR_1 goes off

4- then 2 repeats and so on

- given $V_{B1}(t) = V_{B1}(\infty) - [V_{B1}(\infty) - V_{B1}(0)]\, e^{-t/\tau}$

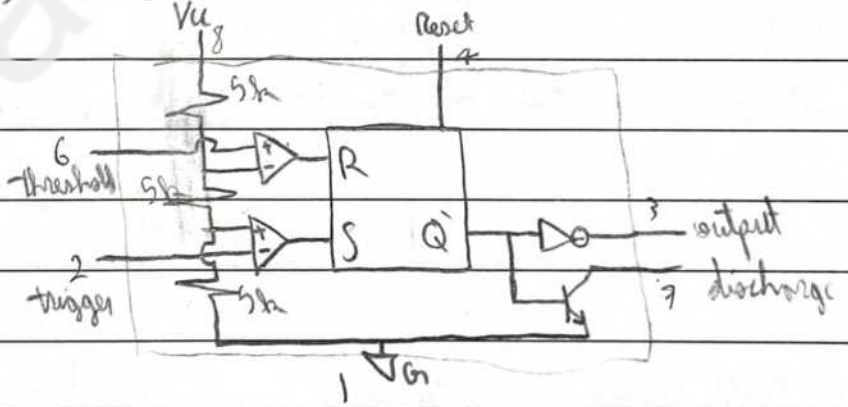
→ time for V_{B1} to equal (0.8V): $T_1 = R_2 C_2 \ln(2)$

∧ $T_2 = R_3 C_1 \ln(2)$ time for V_{B2} to equal 0.8V

∴ $T = R_3 C_1 \ln(2) + R_2 C_2 \ln(2)$

if $R_2 = R_3$ ∧ $C_1 = C_2$ → $T = 2RC \ln(2)$

& 555-timer:



- The open-loop op-Amp can be used as a comparator whose output is high if the voltage at its positive terminal is higher than that at its negative terminal else the output will be low (i.e., negative > positive → output low

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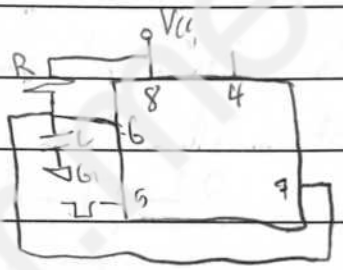
* mono-stable MV using 555:

1- before trigger: $S=0$, $R=0$, $Q=0$, $Q'=1$, transistor is on sat. this state is stable. (is discharged)

2- after trigger: $S=1$, $R=0$, $Q=1$, $\bar{Q}=0$, transistor is (negative trigger) off, C starts charging

3- Remove the trigger before V_c reaches $\frac{2}{3}V_{cc}$: $S=0$, $R=0$, $Q=1$, $\bar{Q}=0$, transistor is off, C will continue charging



4- when V_c exceeds $V_{cc}\cdot\frac{2}{3}$: $S=0$, $R=1$, $Q=0$, $\bar{Q}=1$, transistor is on sat, C will discharge.

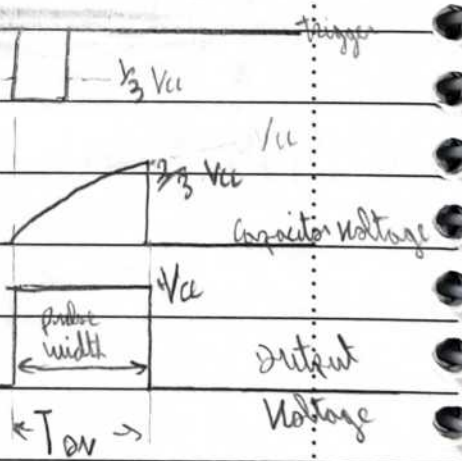
5- when V_c goes below $\frac{2}{3}V_{cc}$: $S=0$, $R=0$, $Q=0$, $\bar{Q}=1$, transistor is on sat, C will fully discharge. This is the stable state of the circuit

$\therefore V_c(t) = V_c(\infty) - [V_c(\infty) - V_c(0)]e^{-t/\tau}$

$\rightarrow V_c(t) = V_{cc}[1 - e^{-t/\tau}]$, $\tau = RC$

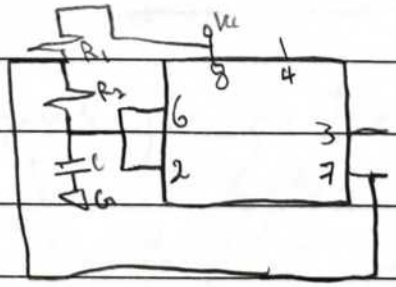
$\therefore V_c(T) = \frac{2}{3}V_{cc} = V_{cc}(1 - e^{-T/\tau})$

$\rightarrow -\ln(3) = \frac{-T}{\tau} \rightarrow T = RC\ln(3)$ 0.1



* Astable MV using 555 timer:

1- assuming the ff is initially Reset, then the transistor will be saturated and the capacitor will discharge to less than $\frac{1}{3}V_{cc}$, which will cause the ff to be set



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2- When the ff is set, $Q = 0$, and the transistor is off hence the capacitor will charge.
at $V_c = \frac{1}{3} V_{cc}$, the output of the S comparator will go low.
and at $V_c = \frac{2}{3} V_{cc}$, the output of the R comparator will go high and the ff will be reset

3- If the ff is reset, the transistor will be on and the capacitor will discharge to repeat the process.

$$V_{c,t}(t) = V_c(\infty) - [V_c(\infty) - V_c(0)] e^{-t/\tau_c}$$
$$\rightarrow V_c(t) = V_{cc} - V_{cc}\left[\frac{2}{3}\right] e^{-t/\tau_c} = 1 - \frac{2}{3} e^{-t/\tau_c}$$
where $\tau_c = (R_1 + R_2) C$

$$\therefore V_{c,d} = V_{cc} - \left[V_{cc} - \frac{2}{3} V_{cc}\right] e^{-t/\tau_d}$$
$$\rightarrow V_{c,d} = V_{cc}\left[1 - \frac{1}{3} e^{-t/\tau_d}\right] \rightarrow \tau_d = R_2 C$$
$T_{on} = (R_1 + R_2) C \cdot \ln(2)$ $\therefore$ $T_{off} = R_2 C \cdot \ln(2)$
$T = T_{on} + T_{off}$ $\rightarrow$ $D = \frac{T_{on}}{T} > 50\%$

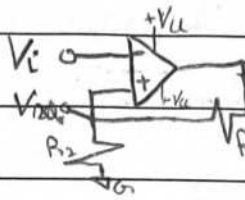
Subject Multivibrators continued Date 24/5/2021 No.

* Multivibrator using Schmitt trigger:

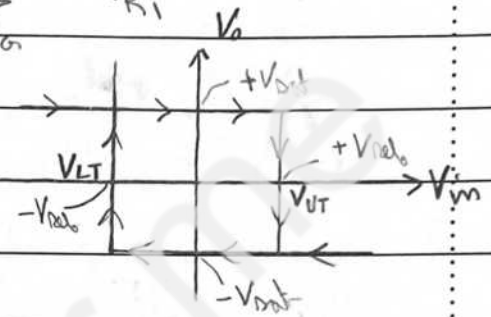
+ Schmitt trigger operation (inverting)

$V_i > V_{ref} \rightarrow V_o = -V_{sat}$

$V_i < -V_{ref} \rightarrow V_o = V_{sat}$



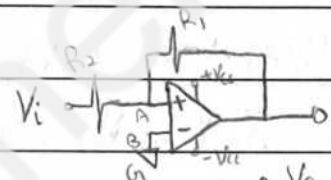
$$V_{ref} = \frac{R_2}{R_1+R_2} \cdot V_o = \begin{cases} \frac{R_2}{R_1+R_2} \cdot V_{sat} = V_{UT} \\ \frac{-R_2}{R_1+R_2} \cdot V_{sat} = V_{LT} \end{cases}$$



- for a low input: $V_o = V_{sat}$

for a high input: $V_o = -V_{sat}$

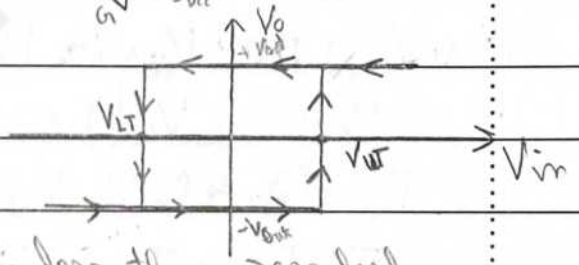
+ Non-inverting Schmitt trigger:



$$V_A = \frac{R_1}{R_1+R_2} \cdot V_i + \frac{R_2}{R_1+R_2} \cdot V_o$$

$$V_B = 0$$

$$V_o = \pm V_{sat}$$



- assuming $V_o = -V_{sat}$ implies that V_A is less than zero for low input, then increase the input until $V_A = 0V$

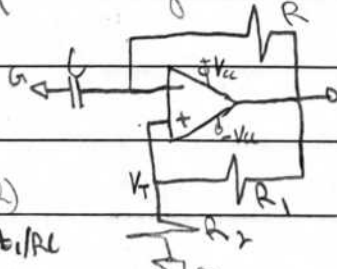
$$\rightarrow V_A = \frac{R_1}{R_1+R_2} \cdot V_i + \frac{R_2}{R_1+R_2}(-V_{sat}) = 0 \rightarrow V_i = V_{UT} = \frac{R_2}{R_1} V_{sat}$$

- hence V_{UT} is low high input that gives $V_o = V_{sat}$
- next set $V_o = V_{sat}$ and decrease the input until $V_A = 0$.

$$V_i = V_{LT} = -\frac{R_2}{R_1} V_{sat}$$

- Therefore, V_{LT} input is the low input that gives $V_o = -V_{sat}$

* Astable multivibrator:



$$V_{c,ch} = V_{sat} - [V_{sat} - (-V_T)]e^{-t/RC} \quad -①$$

$$\text{at } t = t_1, \; V_c = V_T = \frac{R_2}{R_1+R_2} \cdot V_{sat} \quad -②$$

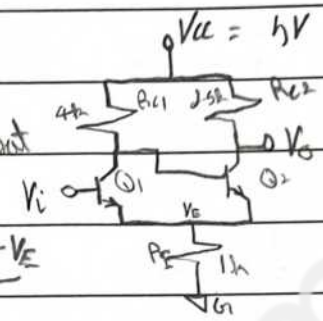
sub ② in ① $\rightarrow$ $V_{sat} - \left[V_{sat} + \frac{R_2}{R_1+R_2} V_{sat}\right] e^{-t_1/RC}$

$$= \frac{R_2}{R_1+R_2} \cdot V_{sat} \quad \therefore t_1 = RC \ln\left(1 + \frac{2R_2}{R_1}\right)$$

Λ $V_{c,fin} = -V_{sat} - [-V_{sat} - V_T]\, e^{-t/RC} = -V_T = \frac{-R_2}{R_1+R_2} V_{sat}$

$\therefore t_2 = RC \ln\left(1 + \frac{2R_2}{R_1}\right)$

& Schmitt trigger using BJT:



$V_{CE,sat} = 0.2V$

$V_{BE,sat} = 0.8V$

- for $V_i = 0$, Q_1 is off and Q_2 must be sat

$\therefore I_E = I_B + I_C = I_{BC2} + I_{RC1} = I_{RE}$

$\rightarrow \frac{V_E}{R_E} = \frac{V_{cc} - V_{BE,sat} - V_E}{R_{C1}} + \frac{V_{cc} - V_{CE,sat} - V_E}{R_{C2}}$

$\therefore V_E = 1.8V \quad \Lambda \quad V_o = 2V$

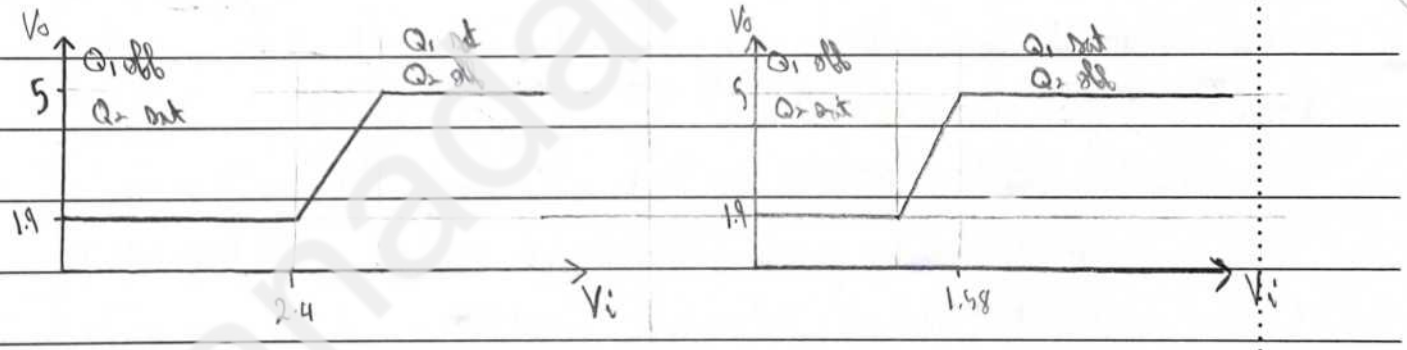
if Q_1 is placed at the edge of conduction by increasing V_i until $V_{BE1} = 0.6V$:

for $V_i > 2.4$, Q_1 will be forward-bias neglecting $I_B \rightarrow I_C = I_E \rightarrow \frac{V_E}{R_E} = \frac{V_{cc} - 0.6 - V_E}{R_{C1}}$

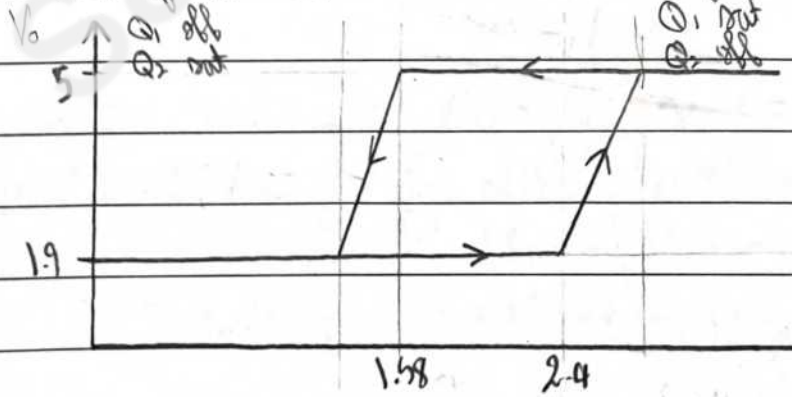
$V_o = V_{cc}$

if Q_2 is placed at the edge of conduction by decreasing V_i until $V_{CE1} = 0.6$

$\therefore V_E = 0.88V \; \Lambda \; V_i = 1.58V$



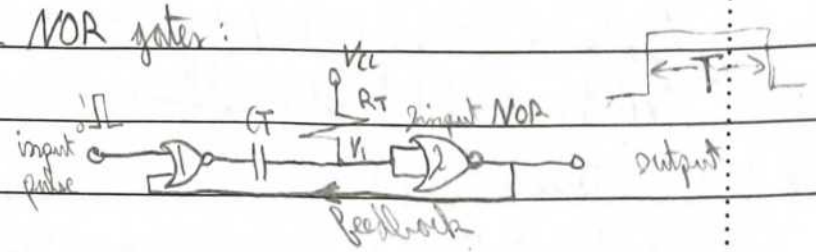
- Combining the above two VTC will give the following hysteresis



hysteresis width = 2.4 - 1.58

Subject multivibrators using gates Date 27/5/2011 No.

Monostable MV using TTL NOR gates:



- if the trigger input is initially low:

Voltage across capacitor $V_{OH} \dashv\vdash V_{cc}$ V_1 → the output from 2 will be low.

- this low input - low output state represents the circuit's stable state.
- when a positive trigger is applied, the output of the first NOR gate will go low and the capacitor will begin to charge through R_T:

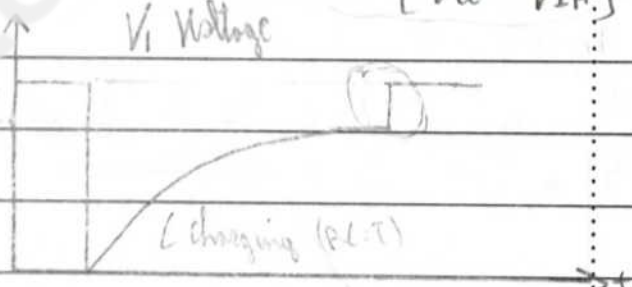
$V_{OL} \dashv\vdash V_{cc} - (V_{OH} - V_{OL})$ ∵ $V_1(t) = V_1(\infty) - [V_1(\infty) - V_1(0)]\, e^{-t/\tau}$, $\tau = R_T C_T$

$\rightarrow V_1(t) = V_{cc} - [V_{cc} - (V_{cc} - V_{OH} + V_{OL})]\, e^{-t/R_T C_T}$

$\therefore V_1(t) = V_{cc} - [V_{OH} - V_{OL}]\, e^{-t/\tau}$

- define T: time for V_1 to equal V_{IH} → $T = R_T C_T \ln\left[\frac{V_{OH} - V_{OL}}{V_{cc} - V_{IH}}\right]$

- the large jump in V_1 voltage occurs when V_1 reaches V_{IH} hence turning the output to NOR 2 low, which is input into NOR 1 causing it to go high. Therefore, the sudden increase in voltage occurs from the capacitor charging through NOR 1.



$V_1 \leq V_{IH}$ $\qquad$ $V_1 > V_{IH}$

$V_{IH} \dashv\vdash V_{IH}$ $\qquad$ $V_{OH} \dashv\vdash V_{IH} + (V_{OH} - V_{IH})$

example: assume $V_{OH} = 3.8V$, $V_{OL} = 0.1$, $V_{IH} = 1.6V$, $R = 15k\Omega$, $C = 1nF$

pulse width: $T = 15 \times 10^{-6} \cdot \ln\left[\frac{3.7}{3.4}\right] \approx 1.27 \times 10^{-6}$ s

Monostable MV using CMOS NOR gates:

∵ $V_{OH} = V_{DD}$, $V_{IH} = V_{DD}/2$, $V_{OL} = 0$

Subject Date No.

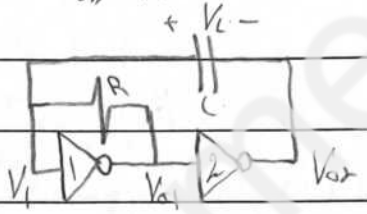
$\rightarrow V_1(t) = V_1(\infty) - [V_1(\infty) - V_1(0)]e^{-t/\tau}$

$\rightarrow V_1(t) = V_{DD} - [V_{DD} - (V_{DD} - (V_{DD} - 0))]e^{-t/\tau}$, $\tau = RC$

$\therefore V_1(t) = V_{DD}[1 - e^{-t/\tau}]$

if $t = T \rightarrow V_1 = V_{IH} \rightarrow T = RC\ln\left(\frac{V_{DD}}{V_{DD} - V_{IH}}\right)$

* Astable MV using inverters:



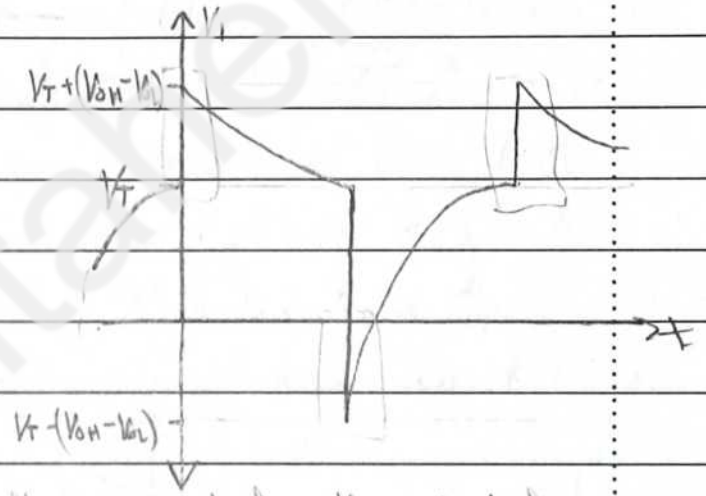
+ two possible states:

1) $V_1 = L \rightarrow V_{o1} = H \rightarrow V_{o2} = L$

2) $V_1 = H \rightarrow V_{o1} = L \rightarrow V_{o2} = H$

- both states are unstable

- assuming $V_{o1} = H$, C will start to charge through R until the transfer voltage (V_T) of inverter 1 is reached, which is registered as a high input and causes V_o to turn low.



- following the large swings in voltage, caused by the output of inverter 2 suddenly turning high, the capacitor will begin to discharge through R, until the voltage (V_1) is low enough to turn the output V_{o1} high. Another jump is seen here as V_{o2} suddenly goes low.

- discharging: $V_{1d}(t) = V_{1d}(\infty) - [V_{1d}(\infty) - V_{1d}(0)]e^{-t/\tau}$

$\rightarrow V_{1d}(t) = V_{OL} - [V_{OL} - (V_T + (V_{OH} - V_{OL}))]e^{-t/\tau}$

$\therefore V_{1d}(t) = V_{OL} - [2V_{OL} - V_T - V_{OH}]e^{-t/\tau}$

define T_1: time at which $V_{1d} = V_T \rightarrow V_{1d}(T_1) = V_T$

$\therefore T_1 = \tau \ln\left[\frac{2V_{OL} - V_{OH} - V_T}{V_{OL} - V_T}\right]$

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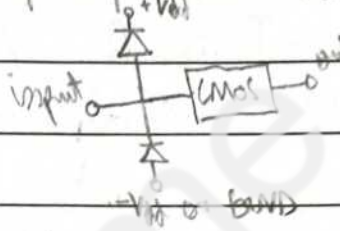
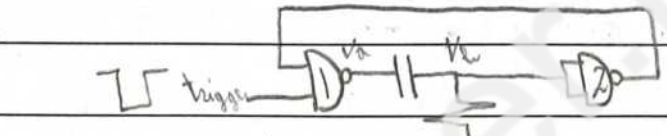
- Charging: $V_{1C}(t) = V_{OH} - [2V_{OH} - V_{OL} - V_T] e^{-t/\tau}$
  - T_2: time at which $V_{1C}(t) = V_T$ $\therefore T_2 = \tau \ln \left[\frac{2V_{OH} - V_{OL} - V_T}{V_{OH} - V_T} \right]$
- If CMOS is used, then the maximum voltage input will be limited to V_{DD} by the protection diodes:



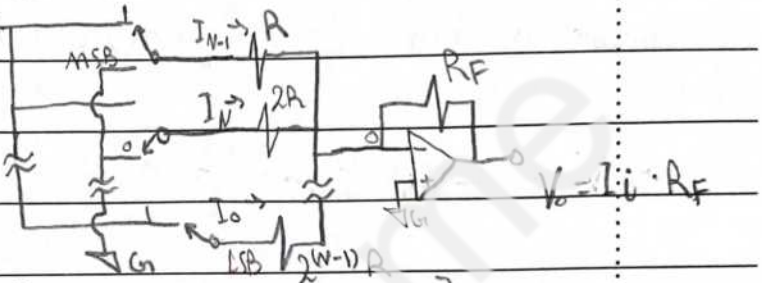
* Monostable using NAND gates:
- the circuit is triggered by a negative pulse and gives a negative pulse at the output.
- the circuit's stable state occurs when the output of V_o is low since the inputs at NAND 1 will be low and high respectively, which will give no change to the output when the circuit is triggered [(low·low)' = high]
- the circuit must be started at the quasi-stable state (V_o = high) so that will allow the circuit to vibrate.



Subject Chapter 9: DACs & ADCs Date 28/5/2011 No.

* DAC: digital to analog converter.
* ADC: analog to digital converter.
+ types of DACs: ① binary weighted, ② R-2R ladder.

① binary weighted DAC:



- if N=4 → $b_3 b_2 b_1 b_0$

$b_{N-1} b_{N-2} \cdots b_1 b_0$

- $V_o = -I_i \cdot R_F = -R_F [I_0 + I_1 + \cdots I_{N-1}]$

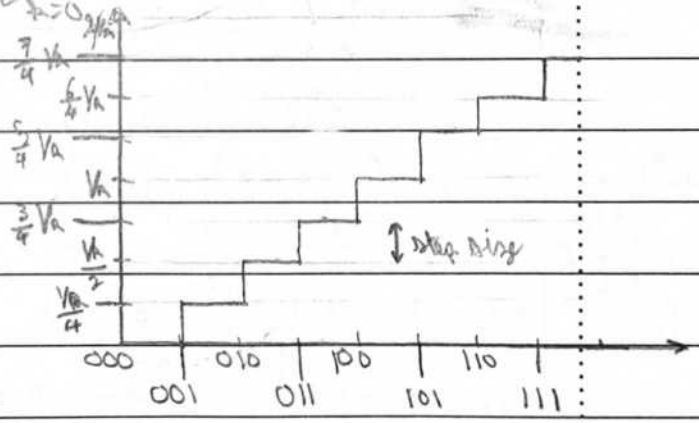
$$= -V_{ref} \cdot \frac{R_F}{R} \cdot \frac{1}{2^{N-1}} \left[\frac{b_0}{2^0} + \frac{b_1}{2^{-1}} + \cdots + \frac{b_{N-2}}{2^{2-N}} + \frac{b_{N-1}}{2^{1-N}} \right]$$

$$\therefore V_o = -V_{ref} \cdot \frac{R_F}{R} \cdot \frac{1}{2^{N-1}} \cdot \sum_{k=0}^{N-1} 2^k \cdot b_k$$

example: $N=3$, $R_F = R$, $V_{ref} = -5V$

$$\rightarrow V_o = 5 \cdot \frac{1}{4} \cdot \sum_{k=0}^{3} 2^k \cdot b_k$$

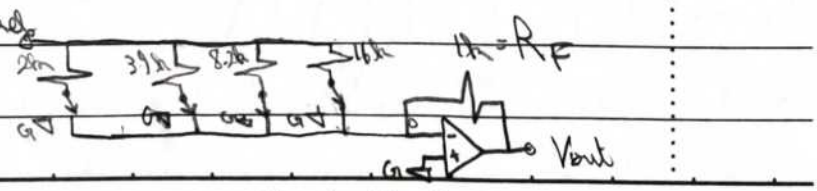
b_2	b_1	b_0	V_o
0	0	0	$\frac{5}{4} V_{ref} = 0$
0	0	1	5/4
0	1	0	5/2
0	1	1	3.75
1	0	0	5
1	0	1	6.25
1	1	0	7.5
1	1	1	8.75



- binary weighted DACs require a wide range of precision-resistors: if N=8 → resistors needed: 2R, 4R, ..., 128R
- resistors should also have low tolerances and low temperature variations

② constant reference current

- another issue with binary weighted DACs is the



large jumps in current passing, which might cause overshoots.
- the circuit shown on the previous page will have a constant current passing through the resistors. based on the switch position, the current will either flow from/to the ground or the R_F.

(2) R-2R ladder DAC:

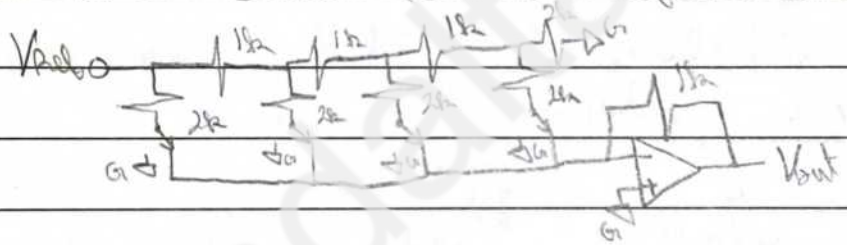
$$\rightarrow V_o = -V_{Ref} \cdot \frac{R_F}{R}\left[\frac{B_0}{16} + \frac{B_1}{8} + \frac{B_2}{4} + \frac{B_3}{2}\right]$$

$$\therefore V_o = -V_{Ref} \cdot \frac{R_F}{R} \cdot \frac{1}{16}\left[2^0 B_0 + 2^1 B_1 + 2^2 B_2 + 2^3 B_3\right]$$

$$\rightarrow V_o = -V_{Ref} \cdot \frac{R_F}{R} \cdot \frac{1}{2^N} \cdot \sum_{n=0}^{N-1} 2^n B_n$$

- the same current issue still stands with the standard R-2R circuit.

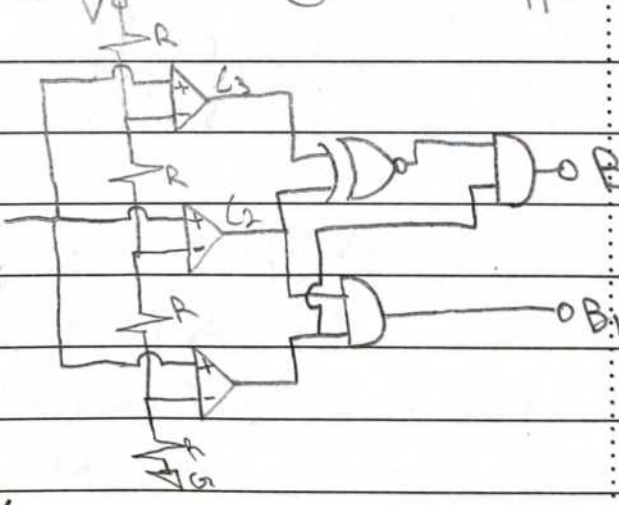
* modified R-2R circuit: (constant reference current)



+ Types of ADCs: (1) parallel or flash converter, (2) successive approximation

(1) 2-bit flash converter:

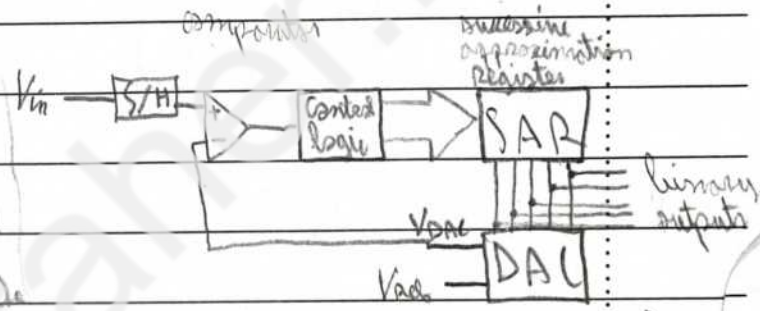
Analog input condition	Comparator outputs			Digital output	
	C_1	C_2	C_3	B_1	B_0
$0 \le V_{in} < \frac{V}{4}$	0	0	0	0	0
$\frac{V}{4} \le V_{in} < \frac{V}{2}$	1	0	0	0	1
$\frac{V}{2} \le V_{in} < \frac{3V}{4}$	1	1	0	1	0
$\frac{3V}{4} \le V_{in} \le V$	1	1	1	1	1



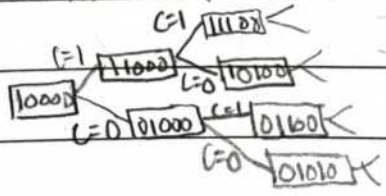
- for an N-bit output, $2^N - 1$ comparators must be used

+ advantages of flash converters:
  - fastest type of ADC since the conversion is performed simultaneously typically taking 100 ns
  - easy to design and construction is simple.
+ disadvantages of flash ADCs:
  - not suitable for large numbers of bits as the number of comparators nearly doubles for every added bit.

(2) Successive approximation ADC:



+ conversion procedure:
  1) start of conversion (SOC) input is set to (1), then the SAR will set the MSB equal to 1 and the rest equal to zero as an initial guess (i.e., for 5 bits: 10000)
  2) the V_{DAC} output is then compared with V_{in}
     - if $V_{in} > V_{DAC}$, the output of the comparator will be (1) and the SAR will maintain the MSB as (1) and set the next bit equal to (1) (i.e., 11000)
     - if $V_{in} < V_{DAC}$, the output of the comparator becomes (0) and the MSB is changed to zero while the second is set to (1) as the second guess (i.e., 01000)
  3) the cycle repeats for all other bits until they have all been tested and set.



example : $N=4$, $V_{Ref} = -5V$, $V_{in} = 3.45V$, DAC: binary weighted, $R=R_0$

$$\therefore V_{DAC} = \frac{-V_{Ref}}{2^{N-1}} \cdot \frac{R_F}{R} \sum_{k=0}^{N-1} 2^k b_k = \frac{5}{8} \sum_{k=0}^{3} 2^k b_k$$

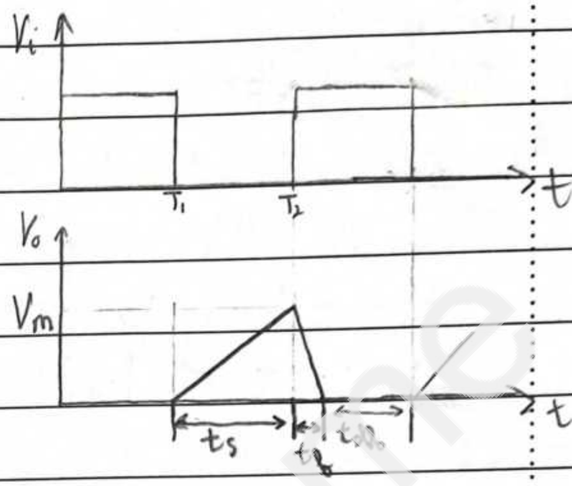
$\therefore$ 1) $b_3 b_2 b_1 b_0 = 1000 \rightarrow V_{DAC} = 5V > V_{in}$ ✓

2) $0100 = 2.5V < V_{in}$ ✓ 3) $0110 = 2.5 + 1.25 > V_{in}$ ✗

4) $0101 \leq V_{in} \rightarrow 3.45 = 0101$ (closest)

Subject: Sweep generators & S&H — Date: 30/5/2021 — No.

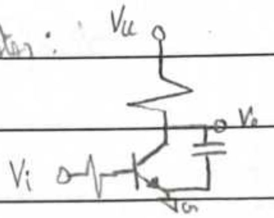
* Sweep circuits:

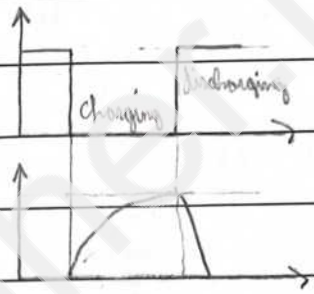


- V_o should be linear as a function of time in interval $T_1 - T_2$

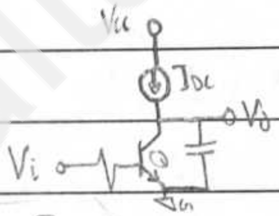
* t_s: sweep time, t_f: flyback time
- t_f should be very small.

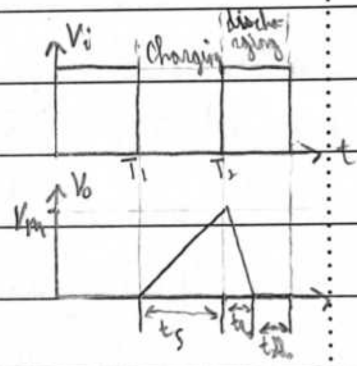
* Sweep circuit with resistor:
- Since the capacitor is charging through a resistor, the output will be exponential.





* Constant current sweep circuit:





- When Q is off: $I_{DC} = C \frac{dV_o}{dt}$

$\rightarrow V_o(t) = \frac{I_{DC}\, t}{C}$

- If Q is saturated: $\beta I_B > I_{DC} + I_{C,dis}$

- When charging: $I_{DC} = C \frac{dV_o}{dt}$

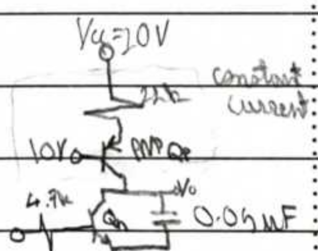
$\rightarrow V_o(t) = \frac{I_{DC}\, t}{C} \rightarrow V_m = \frac{I_{DC}(T_2 - T_1)}{C}$ (max)

- When discharging, Q is forward active:

$I_{DC} = \beta I_B + C\frac{dV_o}{dt} \rightarrow I_{DC} = \beta I_B + C \cdot \frac{(0 - V_m)}{t_f}$

$\therefore t_f = \frac{C V_m}{\beta I_B - I_{DC}}$

Example: Q_P is forward active



∵ Q_P is FA → Voltage on collector terminal is always 0.7V higher than that on the base.

$\rightarrow I_{EP} = \frac{20 - 10.7}{22k} = 0.42273$ mA

∴ $I_{EP} = \frac{\beta+1}{\beta} I_{CP} \rightarrow I_{CP} = 0.4185\ mA$ constant

∴ $I_{CP} = C\frac{dV_o}{dt} \rightarrow V_o = \frac{I_{CP} \cdot t}{C} = 8.37 \times 10^2\, t$

- the maximum output voltage is set to be 10.7V. so the voltage loop across the PNP will become zero then and cause the sweep to plateau.

$\rightarrow V_{om} = 10.7 > \frac{I_{CP}}{C} \cdot t_s \quad \& \quad t_s = T_2 - T_1$

$\therefore \quad t_s < 1.2784\ ms$

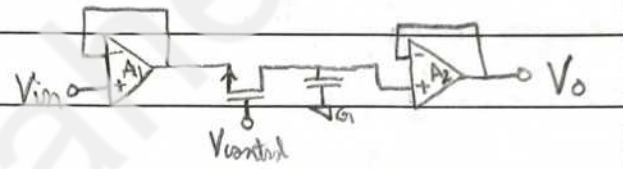
- for discharging: Q_n first goes to forward active

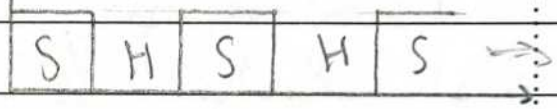
$I_{CP} = \beta_{on} I_{BN} + C\frac{dV_o}{dt} \rightarrow 0.4185\ mA = \beta_0 \cdot I_B + C \cdot \frac{-V_m}{t_R}$

$\therefore \quad t_R = \frac{C \cdot V_m}{\beta_{on} I_{BN} - I_{CP}}$

* Sample & hold:

- Voltage follower op-Amps are used as buffers to eliminate loading effect.
- When active, the mosfet can be modeled as a resistance and it will allow the capacitor to charge and sample the input.
- When the control input is low, the fet will turn off and the input will not be sampled.





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Q1) $T = t_2 + t_1$, $t_1 = R_L \cdot \ln\left(1 + \frac{2R_2}{R_1}\right) =$

$= 1k\Omega \cdot 1\mu F \cdot \ln(1+2) = 1.0986\,ms$

$t_2 = R_L \ln(1+2) \rightarrow f = 0.4551\,kHz$

Q2) Q_2 is always FA $\Rightarrow V_{OH} = -0.7V$

$V_{OL} = -0.7 - I_E \cdot 300$ $\quad I_E = \frac{V_E + 5}{R_E}$, $V_E = V_{ref} - 0.7$

$\Rightarrow V_{OL} = -0.7 - \frac{300}{1240}\left[\frac{V_{OL} - 0.7}{2} - 0.7 + 5\right]$

$\rightarrow V_{OL} = -0.7 - \frac{15}{124} V_{OL} + \frac{15}{124} 0.7 + \frac{15}{620} 0.7 - \frac{15}{62} \cdot 5$

$\rightarrow V_{OL}\left[1 + \frac{15}{124}\right] = \frac{-20.75}{1240} \rightarrow V_{OL} = -1.479V$

$\rightarrow V_{ref} =$

$I_E = \frac{V_E + 5}{1240}$ $\rightarrow V_E = V_{ref} - 0.7$

$\rightarrow I_E = \frac{V_{ref} + 4.3}{1240}$

$-\frac{15}{124} V_{OL} + \frac{15}{124} \cdot 0.7 - \frac{15}{62} \cdot 4.3$

Q4) $T_{on} = RC\ln(3) = 11\,ms$

Q5) V_{IH} , $V_E = -1.4942 \Rightarrow I_E = 2.763\,mA$

$\rightarrow I_{EB} = 1.381\,mA$

Q6) $V_E = 4.5 - 0.7 \rightarrow I_E = 2.923\,mA$

Q9) $V_{SS} = \frac{1 + \frac{\sqrt{2}}{2}\left[V_{DD} - 1\right]}{1 + \frac{\sqrt{2}}{2}} = 2.24264\,V$

$I_{DD} = 60\,mA = k_n (V_{in} - 1)^2 \rightarrow V_{in} = 1.7746$

Q1 $60\,mA = k_p (V_{DD} - V_{in} - 1)^2 \rightarrow V_{in} = 2.90455$

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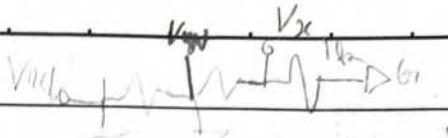
Q12) $V_{ref} = -1.699$

$V_x = \frac{V_{ref}}{4} = -0.1749$



$V_{DC} = \frac{V_{DD}}{2}$

Q13) $V_{TN} < V_i < V_{SS} \rightarrow I_{DQ} = k_n (V_{GSn} - V_{Tn})^2 = k_n (1.5 - 1)^2 = 0.5mA$

Q14) $0.8 - (V_a - 0.1) \leq -6.1V$

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Lafir examples:

2) $V_i = 1.5 \rightarrow V_{Tn} < V_i < V_{SS}$

$\therefore V_{SS} = \frac{1 + \frac{1}{\sqrt{2}}[4]}{1 + \frac{1}{\sqrt{2}}} = -2 + 3\sqrt{2}\ V \approx 2.2426\ V$

$\rightarrow I_{DD} = k_n (V_{GS_n} - V_{Tn})^2 = 0.25 \cdot 100\mu A/V^2 = 25\mu A$

3) $V_{DD} - V_{TL} = 4.4V$

4) $k_R = \frac{k_{driver}}{k_{load}} \Rightarrow V_{SS} = V_{TL} + \sqrt{\frac{1}{k_R}}\, V_{TL}$

$\rightarrow k_R = 9$

5) $V_{OL} = 0.2$, $V_{OH} = 5 \rightarrow P_{OH} = 0$

$V_{OL} = 0.2 \rightarrow I_{OL} = \frac{5 - 0.2}{1k} = 4.8\ mA$

$\rightarrow P_{OL} = 24\ mW \rightarrow P_{Avg} = \frac{P_{OL} + P_{OH}}{2} = 12\ mW$

6) linear mode of operation: $V_{GS} > V_{Tn}$

$V_{DS} < V_{GS} - V_{Tn}$

$\rightarrow V_{GS1} > -2 \wedge V_{GS1} - -2 = 0 - -2 = 2V$

$V_{GS1} - V_{Tn} > V_{DS1} \therefore V_{DS1} = 5 - V_o = 1V$

$\rightarrow$ linear $\therefore I_{DD} = k_n [2(V_{GS} - V_{Tn}) V_{DS} - V_{DS}^2]$

$\rightarrow I_{DD} = 25\mu \cdot [2(2) \cdot 1 - 1] = 75\mu A$

7) $V_o = V(\infty) - [V(\infty) - V(0)] e^{-t/\tau}$

$= 5 - (5 - 0.6) e^{-2} = 4.4045V$

$\rightarrow I = \frac{5 - 4.4045}{10k\Omega} = 59.55\ \mu A$

8) $V_{SS} = 5V$

$V_o = 0.5V \rightarrow$ ~~$V_{SS} < V_i < V_{DD} - V_{TL}$~~ $\rightarrow$ Mp sat

$\rightarrow$ Mn ohmic $\wedge$ Mp sat $V_i = 0$

$\rightarrow I_D = k_p (V_{GSP} - V_{TP})^2 = k_p (5 - 0 - 1.5)^2$

$= 0.245\ mA$

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example 8.8: $T_1 = \tau \ln\left[\frac{2V_{OL} - V_{OH} - V_T}{V_{OL} - V_T}\right]$

$V_{OL} = 0$, $V_{OH} = V_{DD}$ → $\frac{2\cdot 0 - V_{DD} - V_T}{0 - V_T} = \frac{V_{DD}+V_T}{V_T}$

$\therefore T_1 = RC \ln\left(\frac{V_{DD}+V_T}{V_T}\right)$

$\wedge T_2 = \tau \ln\left[\frac{2V_{OH} - V_{OL} - V_T}{V_{OH} - V_T}\right]$ $\wedge V_{OH} = V_{DD}$

$\wedge V_{OL} = 0$ → $\tau \ln\left[\frac{2V_{DD} - V_T}{V_{DD} - V_T}\right]$

$\because R = 10k \wedge C = 1nF$

→ $\tau = 10\,\mu s$ → $T_1 = 10\mu \ln\left(\frac{5+2}{2}\right) = 12.53\,\mu s$

$\wedge T_2 = 10\mu \ln\left(\frac{5-2}{5-5}\right) = 7.81\,\mu s$

$\therefore$ the period is $T = T_1 + T_2 = 22.34\,\mu s$ $\wedge$ duty cycle $= \frac{T_1}{T} = 56.1\%$

if $R = 12k$ → $T_1 = 12\mu \ln(3.5) = 15.03\,\mu s$

$T_2 = 11.77\,\mu s$ → $T = 26.8\,\mu s$

duty cycle $= \frac{15.03}{26.8} = 56.1\%$ same

1) $T_{off} = R_2 C \ln 2$

T_{off} → $V_{c,d} = V(\infty) - (V(\infty) - V(0))e^{-t/\tau_d}$

$V(\infty) = \frac{5\cdot 2}{3} = \frac{10}{3}$ $\wedge V(0) = 0$

→ $V_{c,d} = \frac{10}{3} - \left[\frac{10}{3}e^{-t/\tau_d}\right]$ $\wedge \tau_d = 20k\cdot C$

$V_{c,d} = 0$ → $t = T$

→ $\frac{10}{3} = \frac{10}{3}e^{-t/\tau_d}$ →

$V(0) = \frac{2}{3}\cdot V_{cc} = \frac{10}{3}$ $\wedge V(\infty) = V_{cc}\cdot\frac{20}{30} = \frac{10}{9}$

or $V(T) = \frac{5}{3}$

→ $\frac{5}{3} = \frac{10}{9} - \left(\frac{10}{9} - \frac{10}{3}\right)e^{-T/\tau}$

→ $\frac{\frac{5}{3} - \frac{10}{9}}{\frac{10}{3} - \frac{10}{9}} = \frac{1}{8} = e^{-T/\tau}$ → $T_d = \tau_d \cdot \ln(8)$

$= R_{eq}\cdot C \cdot \ln(8)$

$\wedge R_{eq} = R_1 // R_2 = 14.285$

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(2) $V_{out} = V_{CE2}$

$V_{CE2} = V(\infty) - (V(\infty) - V(0))\, e^{-t/\tau}$

$\therefore \tau = 1k\Omega \cdot 1\mu, \quad V(\infty) = 10$

$V(0) = V_{CE\,sat} = 0 \Rightarrow V_{CE2} = 10 - 10e^{-\frac{t}{\tau}} = 8.65V$

(3) $V_C = \frac{R_2}{R_1+R_2} V_{out} = 2V$

(4) $t_2 = RC \ln\left(1 + \frac{2R_2}{R_1}\right) = RC \cdot \ln(1+1) = RC \ln 2$

(5) $V_{HT} = \frac{R_2}{R_1+R_2} V_{out} = \frac{R_2}{R_1} V_{out} = 3V$

$\therefore V_{LT} = -\frac{R_2}{R_1} V_{out} = -3V$

$\rightarrow$ we are in the hysteresis Region.

$\because$ Voltage is decreasing $\rightarrow + V_{out} = 6V$

examples from slides:

(1) $V_{DD} = 3V, \quad k_n = 150\mu A/V^2, \quad V_{Tn} = 0.5V$

a) $V_o = 0.1$ for $V_i = 3V$

assume linear: $V_o = V_{DD} - R_D k_n \left[2(V_{GS} - V_{Tn}) V_{DS} - V_{DS}^2\right]$

$V_{DS} = V_o \rightarrow 0.1 = 3 - R_D \cdot 150\mu \left[2 \cdot (3 - 0.5) \cdot 0.1 - 0.1^2\right]$

$\rightarrow \frac{2.9}{150\mu} = 0.4 R_D - (0.1)^2 R_D$

$\therefore R_D = 39.455\ k\Omega$

b) transition point: $V_{in} = V_S \quad \wedge V_o = (V_{GS} - V_{Tn})$

$V_{DS} = V_o = V_{DD} - I_D \cdot R_D \quad \wedge V_{GS} = V_S = V_{in}$

$\rightarrow (V_S - V_{Tn}) = 3 - 5.91825 (V_S - V_{Tn})^2$

define $x = (V_S - V_{Tn}) \rightarrow 5.91825 x^2 + x - 3 = 0$

$\rightarrow x = 0.632484 \quad$ or $\quad -0.80145 \quad x = V_o$

$\rightarrow V_S = 1.132484\ V$

example [2]:

V_t: transition from sat to linear, $V_t = \frac{V_T + \frac{V_{DD}}{\sqrt{k_R}}}{1 + \frac{1}{\sqrt{k_R}}}$

1) or $V_t = \frac{V_T\sqrt{k_R} + V_{DD}}{1 + \sqrt{k_R}}$, $k_R = \frac{k_{driver}}{k_{load}} = \frac{k_{n1}}{k_{n2}} = \frac{1}{0.34}$

$\rightarrow V_t = \frac{1.7149859 + 5}{1 + 1.7149859} = 2.4733042\,V$

$\therefore V_{ot} = V_t - V_{Tn} = 1.4733\ldots V$

2) $V_{in} = 5 - 1 = 4V \rightarrow I_D = k_{n2}[2(4-1)V_o - V_o^2]$

$\rightarrow I_D = k_{n1}(V_{DD} - V_o - V_{T1})^2$

$\rightarrow 0.34 \cdot (4 - V_o)^2 = 6V_o - V_o^2$

$\rightarrow 0.34\,(16 - 8V_o + V_o^2) = 6V_o - V_o^2$

$\rightarrow 5.44 - 2.72V_o + 0.34V_o^2 - 6V_o + V_o^2 = 0$

$\rightarrow V_o = 0.698919\,V$

example [3]:

$\because k_n(V_{GS2} - V_{T1})^2 = 3 \cdot k_{n1} \cdot [2(V_{GS1} - V_{T1})V_{DS1} - V_{DS1}^2]$

1) $\because V_{DS1} = V_o \rightarrow (V_{DD} - V_o - V_{T1})^2 = 3[6V_o - V_o^2]$

$\rightarrow 0.34\,(16 - 8V_o + V_o^2) = 18V_o - 3V_o^2$

$\rightarrow 5.44 - 2.72V_o + 0.34V_o^2 - 18V_o + 3V_o^2 = 0$

$\rightarrow V_o = 0.279734\,V$

2) $n = 1$

$\rightarrow 5.44 - 2.72V_o + 0.34V_o^2 - 6V_o + V_o^2 = 0$

$\rightarrow V_o \approx 0.9\,V$

example [4]: all inputs high for low output, $I_D = 1mA$

$V_{oL} = V_{DS1} + V_{DS2} + V_{DS3}$

assume ohmic:

$1mA = k_{n1} \cdot [2(V_{GS1} - V_{T1})V_{DS1} - V_{DS1}^2] \rightarrow \frac{1}{2} = 2(V_{GS1} - 1) \cdot V_{DS1} - V_{DS1}^2$

$\therefore V_{GS1} = V_A = V_{DD} - V_T = 4V$

$\rightarrow -V_{DS1}^2 + 6V_{DS1} - 0.5 = 0 \rightarrow V_{DS1} = 0.084524\,V$

$\wedge \frac{1}{2} = k_n[2(V_{GS2}-1)\cdot V_{DS2} - V_{DS2}^2]$

$V_{GS2} = 4 - V_{DS1} = 3.915476$

$\rightarrow -V_{DS2}^2 + 5.830952 V_{DS2} - 0.5 = 0$

$\therefore V_{DS2} = 0.087049\,V$

$\wedge 2(V_{GS3}-1)\cdot V_{DS3} - V_{DS3}^2 - 0.5 = 0$

$\wedge V_{GS3} = 4 - (V_{DS2} + V_{DS1}) = 3.828427\,V$

$\rightarrow -V_{DS3}^2 + 5.656854 V_{DS3} - 0.5 = 0$

$\therefore V_{DS3} = 0.089843\,V \rightarrow V_{OL} = 0.2614\,V$

$\therefore$ load in saturation sat $\rightarrow I_{mA} = k_n\cdot(V_{GS4} - V_T)^2$

$\wedge V_{GS4} = V_{DD} - V_O = 4.7386\,V$

$\rightarrow k_n = 71.545\ \mu A/V^2$

final exam practice:

1) $V_C = \frac{R_2}{R_1+R_2}\cdot 6 = 2\,V$ [d]

2) $T = R_1 C_1 \ln\left(\frac{V_{OH}-V_{OL}}{V_{CC}-V_{TH}}\right) = 1m\cdot\ln\frac{3.8-0}{5-1.6}$

$V_1(\infty) = 0 \qquad V_1(0) = 0 + (V_{OH} - V_{OL})$

$\rightarrow V_1(t) = V_1(\infty) - [V_1(\infty) - V(0)]\,e^{-t/\tau}$

$\rightarrow V_1(T) = V_{IL} = 0 - [0 - (V_{OH} - V_{OL})]\,e^{-T/\tau}$

$\rightarrow V_{IL} = [V_{OH} - V_{OL}]\,e^{-T/RC}$

$\rightarrow \ln\left[\frac{V_{IL}}{V_{OH}-V_{OL}}\right] = -T/RC$

$\rightarrow T = RC\cdot\ln\left[\frac{V_{OH}-V_{OL}}{V_{IL}}\right]$ NAND ASTABLE

$\rightarrow T = \ln(2.375)\,ms$ = [b]

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[3] if $V_o = 2 \rightarrow V_{DS} = 2V$, $V_{GS} - V_{Tn} = 4V$

→ linear → $I_D = k_n[2 \cdot 4 \cdot 2 - 2^2] = k_n \cdot 12$

→ $I = [C] = 1.2\,mA$

[4] $V_o = 4 \rightarrow$ M_n sat ∧ M_p linear → $I = k_n (V_i - V_{Tn})^2$

$V_i = 0 \rightarrow I = 50\,\mu A$

∧ M_p linear → $I_D = k_p (2(V_{SG_p} - V_{TD}) \cdot V_{SD} - V_{SD}^2)$

∧ $V_{SD} = 1 \rightarrow I_D = 20\mu (2 \cdot 3.5 \cdot 1 - 1^2) = 120\,\mu A$

$V_{oss1} = V_{ss} - V_{Tn}$ ∧ $V_{ss} = \frac{1 + \sqrt{\frac{4}{10}}[5 - 1.5]}{1 + \sqrt{\frac{4}{10}}} = 1.9686\,V$

→ $V_{oss1} = 0.9686\,V$

→ $I_C = 0.12\,mA$ = [B]

5] M_1 : linear → $I_D = k_1[2(0 - V_t)V_{DS1} - V_{DS1}^2] = 0.0439\,mA$

→ [B]

[6] $V_o = 3V$ ∧ $V_{oss1} = V_{ss} - V_{Tn}$ ∧ $V_{ss} = \frac{1 + \sqrt{\frac{3}{5}}[3.5]}{1 + \sqrt{\frac{3}{5}}}$

→ $V_{ss} = 1.9686 \rightarrow V_{oss2} \approx 3.5\,V$

→ $V_o < V_{oss2}$ → M_p out . M_n linear

∴ $I_D = k_p (V_{SG} - V_{TD})^2 = 20\mu[5 - 1.5] =$

$I_D = k_n[2(V_{GS} - V_{Tn})V_{DS} - V_{DS}^2] = k_n[-6 - 9]$

$= -750\,\mu A$ = [A]

[7] $-10 \cdot \frac{R_f}{2R_f}\left[\frac{1}{8} + \frac{1}{4} + \frac{1}{2}\right] = -17.5\,V$ [D]

[8] M_n sat → $I_D = -k_n(5 - 1)^2 = -0.8$ = [D]

[9] 1000 → 1100 ≅ +7.5V → 1010 [C]

[10] [D]

[11] $I_D = C\frac{dV}{dt}$ → $V(\infty) - [V(\infty) - V(0)]e^{-t/\tau}$

[B] → $5 - (5 - 0.6)e^{-2} = 4.4045 = V_C(2\tau)$

→ $I = \frac{5 - 4.4045}{10k} = 59.54\,\mu A \approx 60\,\mu A$

NOTEBOOK

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12 $M_{sat} \rightarrow I_D = k_n (5-1)^2 = 1.6\,mA$ [L]

13 M_n linear $\wedge$ M_p sat $\rightarrow I_D = I_C = k_p (V_{SG_p} - V_{TD})^2$

$\rightarrow I_C = 0.245$ [H]

14 ?

15 $0 \dashv\vdash 0$ [A]

16 $V_{01}(t) = V_{cc} - (V_{cc} - (0.8 - V_{cc} - 0.1))\, e^{-t/R_1 C_1}$

$\wedge t = 0.25T$

$\rightarrow 10 - [10 + 9.2]\, e^{-0.25} = 6.9524\,V$ [L]

17 $\because V_{UT} = \frac{10}{20} \cdot 6 = 3V \wedge V_{LT} = -3V$

still in hysteresis $\rightarrow$ [I]

18 $V_T = \frac{3}{30} = 0.1\,mA \rightarrow \frac{V_{out} = V_x}{10} = 0.1\,mA \rightarrow V_{out} = 4V$

$\rightarrow 4 = 6 - [6+4]\, e^{-t/T} \rightarrow -T/t = \ln \frac{6-6}{10}$

$\rightarrow T = T \cdot \ln(\frac{10}{2}) = T \ln(5)$ [D]

19 $\because V_{GS} = 2.309_4 \rightarrow M_2 \wedge M_D$ sat

$\rightarrow I = k_2 (V_{GS_2} - V_{T_2})^2 = 0.1\,mA$ [L]

20 $-2.5 \quad \frac{-1.25}{1k} = 1.25$ [C]

1 assume $V_{sat} \Rightarrow V_{out} = 4$ [C]

3 M linear $\rightarrow I_D = k_n [2(5-1) \cdot 2 - 2^2] = 1.2\,mA$

$\wedge V \quad 1.2m = C \frac{\Delta V_0}{\Delta t} + \frac{V_{DD} - V_0}{R_D}$

$\rightarrow C \frac{\Delta V_0}{\Delta t} = 1.2m - 0.3 = 0.9$

20 $\frac{V_x}{1k}$

1) $\frac{C dV_o}{dt} + \frac{V_{in} - V_o}{R_0} = I_{in}(G-1)^2 \rightarrow \frac{C dV_o}{dt} = 0$

1) 0.11 → 0.11 (4.3) $I_{B1} = 83.8\,\mu A$

→ $I_{E1} =$ 83.8m

lab exam practice:

1) $t_1 = t_2 \rightarrow f = \frac{1}{2t_1} \wedge t_1 = RC \ln(1+2)$

$\wedge RC = 0.2m \rightarrow t_1 = 0.219\,ms$

→ (e) $f = 2279.59$

2) pulse width $= RC \ln(3) \quad R = R + R_{x1}$

at 1ms: $R = 1820\,\Omega$

at 1.8ms: $R = 3296\,\Omega \rightarrow R_{x1} [0, 1.476\,k\Omega]$

(d)

3) $V_{in} = 4V \rightarrow$ out

4) Q_1 sat: $V_{B1} = 5 - 0.7 = 4.3 \rightarrow I_{B1} = 83.8\,\mu A$

→ $I_{C1} = \beta I_{B1} = 4.19\,mA = I_{B2}$

5) duty cycle $= T_{on}/T \quad V_{UT} = \frac{10}{20} \cdot V_{out} = 6V$

$\wedge V_{LT} = -6V \rightarrow$

$2.4.02\,mA \pm 8.04$

8) $V(\infty) - [V(\infty) - V(0)] e^{-t/\tau} \quad V(0) = 0, \; V(\infty) = 10V$

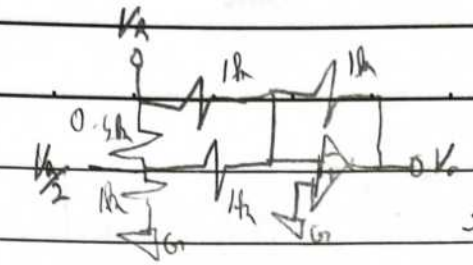
→ $10 - 10 e^{-0.5/\tau} = 4.4$

→ $\tau = 6.4389 \times 10^{-4}$

$\tau = R \times C$

$\tau = 1.58896\,ms \rightarrow R_x =$

9



$$I = \frac{V_A/2}{1k} + \frac{V_A}{1k}$$

$$\rightarrow V_O = 9.45\,V$$

10 $f_s = 15kHz \rightarrow T_{on} + T_{off} = 66.667\,\mu s$

$\wedge$ t3 $(10 + R_B)\cdot C \ln(2) + R_B \cdot C \ln(2) = 66.667\,\mu$

$\rightarrow \ln(2)\cdot C\,[10 + 2R_B] = 66.667\,\mu$

$\rightarrow 10 + 2R_B = 79.2359\,k \rightarrow R_B = 4600\,\Omega$

12 $\ln(2)\cdot C\cdot[R_1 + 2R_2] = \frac{1}{8k}$

$\rightarrow R_1 + 2R_2 = 18.0337\,k\Omega$

$\wedge R_1 + R_2 = 10k \rightarrow R_1 = 1966.3\,\Omega \quad R_2 = 8033\,\Omega$

$\rightarrow T_{on} = (R_1 + R_2)\cdot C \ln(2) = 6.9315 \times 10^{-5}\,s$

$\rightarrow \frac{T_{on}}{T} = 8k \cdot T_{on} = 0.5545$

13 $R_T = R + 50k$

$\rightarrow T_{max} =$

14 $T_{on} = 0.64 \cdot T$

$\wedge T_{on} = 20k \cdot 0.05\mu \cdot \ln(2)$

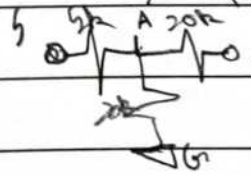
$\wedge T = T_{on} + R_B \cdot 0.05\mu \cdot \ln(2)$

$\rightarrow \left(\frac{1}{0.64} - 1\right) T_{on} = R_B \cdot 0.05\mu \cdot \ln(2)$

$\wedge T_{on} = 6.93147 \times 10^{-4}\,s$

$\rightarrow R_B = 11250\,\Omega$

18



$$\rightarrow \frac{5 - V_A}{5k} = \frac{V_A}{20k} + \frac{V_A + 12}{20k}$$

$$\rightarrow 20 - 4V_A = V_A + V_A + 12$$

$$\rightarrow 6V_A = 8 \rightarrow V_A = \frac{4}{3}\,V$$

(19) $V_{in} = 0 \rightarrow V_o = \text{high}$

$I_{RL} = n \cdot \frac{5.2294 - 0.8}{10k} = \frac{5 - 3.2294}{1k}$

$\rightarrow n = 9$

examples continued:

example 1: $V_{SS} = V_{T1} + \sqrt{\frac{k_L}{k_1}} \cdot V_{TL}$

$\wedge V_{OSS}^2 = \frac{k_L}{k_1} V_{TL}^2$

$\rightarrow V_{SS} = 1 + \sqrt{\frac{0.2}{1}} \cdot (-1) = 1 \mp \frac{\sqrt{5}}{5}$

$\rightarrow V_{SS} = 0.553\text{V}$ or 1.4472V

$\wedge V_{OSS} = \pm\sqrt{0.2}\,(-1)^2 = 0.447\text{V}$

$I_D = k_1 (V_{SS} - V_{T1})^2 \approx 0.2\text{ mA}$

for V_{o2}: $2(V_i - V_{T1}) \cdot V_{o2} - V_{o2}^2 = 0.2 \cdot (V_{OSL} - V_{TL})^2$

$V_i = V_{DD} \wedge V_{OSL} = 0$

$\rightarrow 2(4) \cdot V_{o2} - V_{o2}^2 = 0.2$

$\therefore V_{o2} = 0.025079\text{V}$

11 $0.1\text{k} \cdot \ln(2) \cdot 8\text{k} =$

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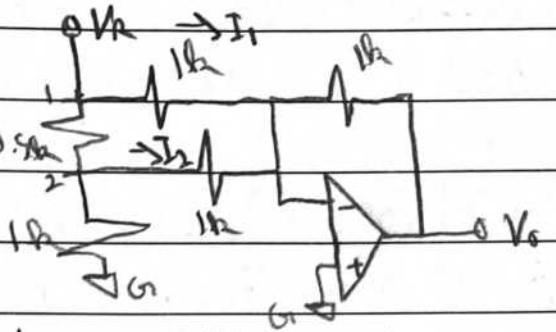
12) $T_{on} = (R_1 + R_2)\, C \cdot \ln 2 \quad \wedge \quad R_1 + R_2 = 10\text{k}$

$T_{total} = \frac{1}{8\text{k}}$, duty cycle $= \frac{T_{on}}{T_{total}} = T_{on} \cdot 8\text{k}$

$\rightarrow$ duty cycle $= 0.55452$

10)



$I_1 = \frac{V_A}{1\text{k}}$

$I_2 = \frac{V_2}{1\text{k}} \wedge V_2$

5) $V_{UT} = 4V \wedge V_{LT} = -4V$

$0 \rightarrow \frac{-4}{10}$

$0 \rightarrow 2.572 \times 10^{-3} \rightarrow t_{xtb} = 5.144\ ms$

$T = t \rightarrow T_{on} = 5.926 - 5.144 = 0.782$

$\rightarrow D =$

$t\_V_{UT} = \ln\left(\frac{4}{10}\right) / 160 \rightarrow t_{on} =$

16) $V_A > V_{in}$

$\frac{5 - V_{neb}}{5\text{k}} = \frac{V_{neb}}{20\text{k}} + \frac{V_{neb} - V_{out}}{20\text{k}}$

$\rightarrow 20 - 4V_{neb} = 2V_{neb} - V_{out}$

$\rightarrow 6V_{neb} = 20 + V_{out}$

$\therefore V_{neb} = \frac{20 + V_{out}}{6}$

18) when $V_A = V_{in} \wedge V_o = -V_{out} \rightarrow$

$V_A = V_{in}$

$\frac{V_{in}}{20\text{k}} = \frac{V_x - V_{in}}{5\text{k}} - \frac{V_x - V_o}{20\text{k}}$

$\rightarrow V_{out} = 12$

$\rightarrow V_{neb} = \frac{32}{6} =$

$V_{in} = 4V_x - 4V_{in} - V_x + V_{out} \rightarrow V_{in} =$

$V_{neb} = 4V_x - 4V_{neb} - V_x - V_o$

$\rightarrow V_{neb} = \frac{5V_x - V_o}{5}$

example:

1) $k_L(V_{GSL} - V_{TL})^2 = m\, k_{n1} V_{DS1}\left[2(V_{GS1} - V_{T1}) - V_{DS1}\right]$

$\rightarrow 0.34 = 3\cdot\left[2(4)\cdot V_{OL} - V_{OL}^2\right]$

$\rightarrow 3V_{OL}^2 - 24V_{OL} + 0.34 \Rightarrow V_{OL} = 0.0142\ V$

2) $V_{OL}^2 - 8V_{OL} + 0.34 = 0 \rightarrow V_{OL} = 0.0423\ V$

example

1) $I_D = 1mA$

$\Rightarrow 1mA = 2\times10^{-3}\left[2(V_{GS1} - V_T)V_{DS1} - V_{DS1}^2\right]$

$\rightarrow 0.5 = 2(5-1)\cdot V_{DS1} - V_{DS1}^2$

$\therefore V_{DS1} = 0.063\ V$

$1mA \rightarrow 0.5 = \left[2(5 - V_{DS1} - 1)V_{DS2} - V_{DS2}^2\right]$

$\rightarrow V_{DS2} = 0.063\ V$

$\therefore 0.5 = 2(5 - V_{DS1} - V_{DS2} - 1)V_{DS3} - V_{DS3}^2$

$\rightarrow V_{DS3} = 0.063\ V$

$\therefore V_{OL} = 0.1921\ V$

$\because M_L$ saturation $\rightarrow 1mA = k_L \cdot V_{DSL}\left[2(0+1) - V_{DSL}\right]$

$\therefore 1m = k_L\left[2(4.8079) - 4.8079^2\right]$

$\rightarrow k_L =$ negative ✗

$\because V_{DSL} > V_{GSL} - V_{TL} \rightarrow M_L$ sat

$\therefore 1mA = k_L(V_{GSL} - V_{TL})^2 \Rightarrow k_L = 1mA$

Question 3:

1) $\because V_{OL} \rightarrow M_L$ sat & M_D active

$I_D = k_L(V_{GSL} - V_{TL})^2 = k_D V_{OL}\left[2(V_{GSD} - V_{TD}) - V_{OL}\right]$

$\rightarrow 1 = 3.2\left[8V_{OL} - V_{OL}^2\right]$

$\rightarrow V_{OL} = 0.03924$

5) $\because V_{UT} = \frac{10k}{10k+20k} \cdot V_{out} \rightarrow V_{UT} = 4V$

$\therefore V_{LT} = \frac{1}{3}(-V_{out}) \rightarrow V_{LT} = -4V$

assume starting at $t=0$

V_{in} reaches V_{UT} then returns to 0

t_{UT}: $V_{UT} = V_{in} = 10\sin(160t) \rightarrow t = \frac{\sin^{-1}(\frac{4}{10})}{160}$

$\rightarrow t_{UT} \approx 2.572$ ms

$\therefore t_{on} = 2t_{UT}$

$\therefore t_{LT}$: $V_{LT} = -4 = 10\sin(160t) \Rightarrow |t_{LT}| = 2.572$ms

$\therefore t_{off} = 2t_{LT}$

$T = t_{off} + t_{on}$; duty cycle $= \frac{t_{on}}{T}$

$\because T = 2t_{on} \rightarrow D = 50\%$

1) $V_{in} = 5V$ M_1 is linear and M_2 is sat

$\rightarrow k_1 \cdot V_{o1}[2(4) - V_{o1}] = k_2(1)^2$

$\rightarrow \frac{k_1}{k_2} = 8V_{o1} - V_{o1}^2$

2) $V_{gs1} = V_{Tn}$ $\therefore V_{DD1} = V_{DD} \rightarrow NM_H = 3.41V$

3) $\because V_{SS} = \frac{1 + \frac{20}{20}[V_{DD} - 1.2]}{1 + \frac{1}{3}} = \frac{1 + \frac{1}{3}[3.8]}{4/3} = \frac{3 + 3.8}{4} = 1.7$

$\therefore V_{in} < V_i < V_{SS} \rightarrow M_n$ sat $\therefore M_p$ linear

$\therefore I_D = k_n(V_{GSn} - V_{Tn})^2 = 47.628\,\mu A$

$\therefore P_{dissipated} = 238.4\,\mu W$

(A) M_2 always sat

$\therefore k_2 (V_{DD} - V_o - 1.2)^2 = k_{2D} (V_{in} - 0.8)^2$

$\rightarrow k_2 / k_{2D} = 1.96 \rightarrow$

or $V_o = V_{DD} - V_{T2} - \sqrt{\frac{1}{1.96}} \cdot (V_{in} - V_{T1})$

$\rightarrow V_o = 4.2 - \frac{5}{7}[V_{in} - 0.8]$ at $V_{T1} < V_{in} < V_{DS} + V_{TD}$

$\therefore V_t =$

$\therefore 2.45 < V_o < 4.2$

Assume $V_{in} = V_{DS} + V_{TD} \rightarrow V_o = 4.2 - \frac{5}{7}[V_t]$

$\rightarrow V_o = 2.45$

$V_{GSL} = 5 - V_o$, $V_{DSD} = V_o$, $V_{GSD} = V_{in}$

$\therefore M_D$ sat $\rightarrow 0.8 < V_{in} < V_t$

find V_t : $k_{n1} (V_t - 0.8)^2 = k_{n2} (V_{DD} - V_{ot} - V_{T1})^2$

$k_R = \frac{k_{driver}}{k_{load}} \rightarrow 1.96 (V_t - 0.8)^2 = (V_{DD} - V_t + 0.8 - 1.2)^2$

$\rightarrow \sqrt{1.96} (V_t - 0.8) = (V_{DD} - V_t - 0.4)$

$\rightarrow 2.4 V_t - 1.12 = 5 - 0.4$

$\rightarrow V_t = 2.38333 \ldots V$

If $V_{in} = V_t \rightarrow V_o = 1.9833$

$\frac{5}{7} V_t - 1.12 = 4.6 - V_t$

$\rightarrow 2.4 V_t = 5.72$

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[4] M_1 always sat ∧ M_D sat

→ $V_{TD} < V_{in} < V_t$ check range 22 ch prob's slides

∧ $V_o = V_{DD} - V_{TL} - \sqrt{k_R}(V_{in} - V_{TD})$ (Ch-7)

∵ $k_D (V_t - V_{TD})^2 = k_L (V_{GSL} - V_{TL})^2$

∧ $V_{GSL} = V_{DD} - V_{ot}$ ∧ $V_{ot} = V_t - V_{TD}$

→ $k_R (V_t - 0.8)^2 = (V_{DD} - V_t + 0.8 - 1.2)^2$

→ $\frac{3}{5}(V_t - 0.8) = 4.6 - V_t$

∴ $V_t = 2.38333\ldots V$

at $V_{in} = V_{TD}$, $V_o = V_{DD} - V_{TL} = 3.8V$

at $V_{in} = V_t$, $V_o = 1.58336V$

∴ $1.5833\overline{6}V < V_o < 3.8V$

[1] ∵ $V_{SS} = V_{TD} \pm \sqrt{\frac{k_L}{k_D}} \cdot V_{TL}$

→ $1.6 = 1 \pm \sqrt{\frac{1}{k_R}} \cdot (-1.2)$

→ $\sqrt{k_R} = 2$ → $k_R = 4$

[3] $V_{IL} < V_{Tn}$ → $NM_L = V_{Tn} - V_{OL} = V_{Tn}$

[6] $2.9 = V_{IH}$ ∧ $1.2 = V_{IL}$

$NM_L = 1.2 - 0.2 = 1$

[7] $V_{DD} - V_{Tn} = 4V$

[8] $V_{SS} = \frac{V_{Tn} + \sqrt{\frac{1}{2}}[5-1]}{1 + \frac{1}{12}} = 2.42604V$

→ $V_{DD} - V_t < V_i < V_{DD}$ → M_p off ∧ $V_o = 0$

→ $V_{OSL} = -V_{SDL} = -5$

9 $P_{OH} = 0$ $P_{OL} = \frac{4.5}{10} \cdot 5 = 22.5\ mW$

$\rightarrow P_{avg} = \frac{P_{OH} + P_{OL}}{2} = 11.25\ mW$

10 $V_{in} = 0.3 \rightarrow M_1$ off $\rightarrow V_o = V_{DD}$

$\rightarrow V_{DSL} = 0$

11 $V_{TD} < V_{in}$ $\because V_{SS} = V_{TL} \pm \sqrt{\frac{1}{k_R}} V_{TL}$

$\rightarrow V_{SS}$ $\because V_{GS1} > V_{TH}$ & $V_{DS1} = V_o > (V_{GS} - V_t)$

$4.6 > 0.2 \rightarrow M_1$ sat

$\because V_{DSL} = 0.4 < 0 - V_{TL} \rightarrow M_L$ is linear

13 $V_{in} = 1.8$, $\sqrt{k_R}(V_t - 0.8) = (V_{DD} - 0.4 - V_t)$

$\rightarrow 1.2 V_t = 5.4\ V \rightarrow V_t = 2.7\ V$

$\therefore$ $V_{TD} < V_{in} < V_t \rightarrow M_1$ is sat

no need to calculate V_t since we know it is larger than V_{in} so both transistors are sat

$\rightarrow V_o = V_{DD} - V_{TL} - \sqrt{k_R}(V_{in} - V_{TD})$

$\rightarrow V_o = 2.8\ V$

14 $\because V_{SS} = \frac{V_{TH} + \frac{1}{2}[A]}{1.5} = 2$

$\rightarrow V_{TD} < V_{in} < V_{SS} \rightarrow M_n$ sat, M_p triode

$\rightarrow I_D = k_n (V_{in} - V_{TH})^2 = \frac{k_n}{4} = 50\mu A$

15 $V_{DD} - V_{TL} = 5 - 0.8 = 4.2\ V$

---

1 $\frac{V_o - V_{ref}}{R_1} = \frac{V_{ref} - V_x}{R_2} \rightarrow V_o - V_{ref} = 2V_{ref} - 2V_x$

$\rightarrow V_o + 2V_x = 3V_{ref} \rightarrow V_{ref} = 4$

[2] $V_L(t) = V_L(\infty) - [V_L(\infty) - V_L(0)]e^{-t/\tau}$

T: time until $V_L = V_{IL} = 1.6$

$\rightarrow 1.6 = 0 - [0 - 3.8]e^{-T/RC}$

$\rightarrow \frac{1.6}{3.8} = e^{-T/RC} \rightarrow \ln(\frac{3.8}{1.6}) = \frac{T}{RC}$

$\therefore T = ms \ln(2.375)$

[3] $\because V_{GS} = V_i = 5V \wedge V_{DS} = V_O = 2V$

$\rightarrow 2 < 5 - V_{TN} \rightarrow$ linear

$\therefore I_D = k_n V_O(2(V_{GS} - V_{TN}) - V_O)$

$\rightarrow I_D = 1.2mA = C\frac{\Delta V_O}{\Delta t} + \frac{V_{DD} - V_O}{R_D}$

$\rightarrow C\frac{\Delta V_O}{\Delta t} = 0.9mA$

[4] $\because V_{SS} = \frac{1 + \left[\frac{2}{5}(5 - 1.9)\right]}{1 + \frac{1}{5}} = 1.9685607$

$\rightarrow V_{OSS2} = 3.6685h$

$\because V_{OSS2} < V_O \rightarrow M_n$ off $\wedge M_p$ linear

$\therefore I_D = I_L = k_p V_O(2(V_{SG} - V_{tp}) - V_O)$

$\rightarrow I_D =$

$I_D = k_p V_{SDP}[2(V_{SGP} - V_{TP}) - V_{SDP}]$

$\wedge V_{SGP} = 5V \wedge V_{SDP} = 1$

$\rightarrow I_D = k_p[7 - 1] = 120\mu A$

[5] M_D linear $\wedge M_L$ sat M_D sat $\wedge M_L$ linear

$I_{DD} = k_n(V_{GS} - V_{TD})^2 = 75\mu A$

$\wedge I_{DL} = k_L(4 \cdot 0.5 - 0.5^2) = 0.0437.5$

Check V_{DS} on M_D

$4.5 > -V_{TN}$

$\because V_{DSL} = 0.5 < 0 - -2 \rightarrow$ linear

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[6] $V_{SG} = 1.969 \Rightarrow |V_{TP}| < V_{SG}$

M_n linear $\wedge$ M_p sat X M_p cutoff since $V_{SG} < |V_{TP}|$

$I_C = I_{Dn} - I_{Dp}$

$\wedge I_{Dn} = k_n(8-3-3^2) = 750\ mA$

$\wedge I_C = I_{Dn} = -750\ mA$

[7] $V_{out} = 10V \rightarrow V_o = -10 \cdot \frac{40k}{20k}\left(\frac{1}{8}+\frac{1}{4}+\frac{1}{2}\right)$

$\rightarrow V_o = -17.5V$

[8] M_p cutoff, M_n sat

$\rightarrow I_D = k_n(5-1)^2 = 0.8\ mA$

[9] 1000 : $-V_{out} \cdot \frac{R_b}{R} \cdot [\ ] = 5$

$\because 6.5 > 5 \rightarrow$ end of first cycle = 1000

next 1100 : $-V_{out} \cdot 1.5 = 7.5$

$\because 6.5 < 7.5 \rightarrow$ comparator output = 0

$\rightarrow$ end of second cycle : 1010

[10] $V_t = \frac{V_{DD}}{3} = 1.667V$

[11] $V_o(t) = V_o(\infty) - [V_o(\infty) - V_o(0)]\, e^{-\frac{t}{\tau}}$

$\rightarrow 5 - (5-0.6)\, e^{-2} \rightarrow V_o(1) = 4.594V$

$\rightarrow I_C = 59.54\ mA \approx 0.06mA$

[12] $I_D = I_C + \frac{V_{DD} - V_o}{R_D}$

$\wedge$ as $V_{DS} = 4.5 > V_{GS} - 1 \rightarrow$ sat

$\rightarrow I_D = k_n(4)^2 = 1.6\ mA$

$\rightarrow I_C = 1.55\ mA$

[13] M_n cutoff $\wedge$ M_p sat $\because V_o < V_{TP}$

$\rightarrow I_C = I_{DP} = k_p(V_{SGP} - |V_{TP}|)^2$

$= 20u[5-1.5]^2 = 0.245mA$

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16 $V_0(t) = V_0(\infty) - [V_0(\infty) - V_0(0)]\, e^{-t/\tau}$

$\Rightarrow V_0(0.25T) = 10 - [10 + 0]\, e^{-0.25}$

assuming trigger at $t = 0^+$ $\Rightarrow 10(1 - e^{-0.25}) =$

$V_0(0) =$

at $t = 0 \Rightarrow Q_2$ switches from sat to cut

$\Rightarrow t = 0^- \Rightarrow Q_1$ sat

$\therefore V_0(0) = 0.8 - 10 = -9.2\ V$

$V_{BE\,sat} - (V_{CE\,sat} - V_{\gamma}) \;|\!-\; V_{CE\,sat} - V_{CC}$

$\therefore V_0(0.25T) = 10 - [10 + 9.2]\, e^{-0.25}$

$= -4.43\ V$

18 $\dfrac{V_{reb} - V_x}{R_2} = \dfrac{V_o - V_{reb}}{R_1} \Rightarrow 2V_{reb} - 2V_x = V_o - V_{reb}$

$\Rightarrow 3V_{reb} = 6 + 6 \Rightarrow V_{reb} = 4$

$\Rightarrow t_{on} \Rightarrow V_c = V_{reb} - V_{sat} - (V_{sat} + V_T)\, e^{-t_{on}/RC}$

$\Rightarrow \dfrac{2 - 4}{2 + 4} = e^{-t_{on}/RC}$

$\Rightarrow t_{on} = RC \ln\left(\dfrac{V_o}{6}\right)$

19 assume M_2 sat $\Rightarrow I_C = I_L$

$\therefore V_{DS_L} = 3V > |V_{TL}| \Rightarrow M_2$ sat

$\Rightarrow I_C = I_L = k_n (0 + 2)^2 = 100\ mA$

18 $V_{reb} = V(\infty) - [V(\infty) - V(0)]\, e^{-t/RC}$

$\Rightarrow V(t_{on}) = V_{reb} \wedge \dfrac{V_{reb} - 3}{10k} = \dfrac{6 - V_{reb}}{20k}$

$\Rightarrow 2V_{reb} - 6 = 6 - V_{reb} \Rightarrow V_{reb} = 4V$

$\Rightarrow V_{c,ch}(t) = 6 - [6 + 4]\, e^{-t/RC}$

$\Rightarrow \ln\left(\dfrac{6 - 4}{6 + 4}\right) = \dfrac{-t_{on}}{RC} \Rightarrow t_{on} = RC \ln\left(\dfrac{10}{2}\right)$

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Q1) $\frac{V_{ref} - V_x}{R_2} = \frac{V_o - V_{ref}}{R_1}$

$\rightarrow \frac{V_{ref} - 4.5}{10.7} = \frac{9 - V_{ref}}{20.5}$

$\rightarrow 1.9158\, V_{ref} = 9 + 4.5 \cdot \frac{20.5}{10.7}$

$\rightarrow V_{ref} = 6.0A$

Q2) $V_{DS} < V_{GS} - 1 \rightarrow$ linear

$\therefore I_D = I_L + I_L$ ، M_1 is sat

$\rightarrow I_L = k_L (0 + 2)^2 = 0.168\ mA$

، $I_D = k_n (8 \cdot 1.8 - 1.8^2)$

$\rightarrow I_D = 8.91686 \times 10^{-4}$

$\rightarrow I_L = 74.88\ \mu A$

Q3) $V_x = 0V \rightarrow t_{on} = RC \ln\left(1 + \frac{2R_2}{R_1}\right)$

، $t_{off} = t_{on}$

$\rightarrow t = 2 \cdot 1.43\, m \ln$

$\rightarrow t = 1.9460\ ms$

$\rightarrow f =$

Q4) 1.76 V 5.6V

Q5) $-V_{ref} \cdot \frac{R_f}{R} \cdot \left(\frac{1}{8} + \frac{1}{4} + \frac{1}{2}\right) =$

Q6) $I =$ (2) $I_{op\text{-}amp} =$

Q7) $Q_2(t=0) =$ not ، $Q_2(t=0) =$

$\rightarrow V_{o2}(t) = V(\infty) - [V(\infty) - V(0)] e^{-t/RL}$

$V(\infty) = 0.8 \rightarrow V_{o2}(2.1T) = 0.8 - (0.8 - 10) e^{-2.1}$

$\rightarrow V_{o2} =$

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$V_o = 0.8 - V_{tn}$ V_o

Δ $V_o(2.1\tau) = 10 - (10 + 10 - 0.8)\, e^{-2.1}$

$\rightarrow V_o = 8 - (8 + 7.2)\, e^{-2.1} = 6.1387$

Q2) M_D off $\therefore$ $V_{DS1} = 3.2 \rightarrow M_1$ in sat

$I_D = I_C = k_1 (0 + 2)^2 = 0.1148$ mA

Q9) $t = 2\tau \rightarrow V_c = V_{01} - (V_{01} - V_{DD})\, e^{-2}$

$\therefore$ $V_{01} =$ ~~$\times$~~ 0.45 V

$\rightarrow V_c = 1.06597$

$\therefore$ M in linear $\rightarrow I_D = k_n (8 V_o - V_o^2)$

$\rightarrow I_D = 0.739$ mA

$I_D = I_C + I_R$ Δ $I_R = \frac{5 - V_o}{10.9\,k}$

$\rightarrow I_C =$

low $\rightarrow$ high

$V_c(\infty) = V_{01}$ $V(\infty) - (V(0) - V(0^-))\, e^{-2}$

$\rightarrow V(2\tau) =$

4.384 V $\rightarrow$

Q10) $V_{in}(\infty) = 0.48$ V.

$\rightarrow 0.08 - (0.48 - 0)\, e^{-T/\tau}$

$\rightarrow 0.48 e^{-T/\tau} = 0.48$

$\rightarrow T =$

$0.48 V_{DD} -$

$0.48 V_{DD} = 0 - (0 - V_{DD})\, e^{-T/\tau}$

$\rightarrow e^{-T/\tau} = 0.48$

$\rightarrow T = \tau \ln \frac{1}{0.48} = 0.73$

Q11) M_3 is sat $\rightarrow I_D = k_n (4)^2 = 1.312\ mA$

$I_L = k_n (.2 \cdot 0.2 - 0.2^2) = 10.368\ mA$

Q12) $I_L = -k_n (V_{DD} - V_{TN})^2$

Q13) $V_{B2}(\infty) = 8$

$-11 + 10$

$8 - (8+10) e^{-0.4}$

$0.8 - 0.8 + 10$

$V_{B2}(0) = 0 \quad \& \quad V_{B2}(\infty) = 10$

Q14) $I_D = I_L + I_{D3}$

Q15) $T_{low} = (R_1 + R_2) C \ln 2$

$\& \quad D > 50\% \rightarrow \frac{(R_1 + R_2) \cdot C \ln 2}{(R_1 + R_2 + R_2) C \ln 2}$

$\rightarrow \frac{R_1 + R_2}{R_1 + 2R_2} > 50\%$

$19.6\ k\Omega \rightarrow R_1 + R_2 \geq 0.5 R_1 + R_2$

$\rightarrow 0.5 R_1 >$

$\frac{R_1}{R_1 + R_2} = \frac{2}{3} D$

Q16) $V(\infty) = \frac{V_{cc}}{3}$

$\frac{V_{cc}}{3} = 0 - \frac{V_{cc}}{3} e^{-t/\tau}$

$\rightarrow \frac{V_{cc}}{3} = V_{cc} - V_{cc}\left(1 - \frac{1}{3}\right) e^{-t/\tau}$

$\rightarrow \frac{1}{3} = 1 - \frac{2}{3} e^{-t/\tau}$

$T = \quad \frac{1}{3} = 1 - e^{-t/\tau} \rightarrow T =$

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$\frac{2}{3} = 1-(1-\frac{1}{3})e^{-} \rightarrow \frac{1}{3} = \frac{-2}{3}e^{-}$

$\rightarrow T = \dots$

Q18) at V_{ss} : $V_{ss} = \frac{1+\sqrt{\frac{63}{228}}(5-1.5)}{1+\sqrt{\frac{63}{228}}} = 1.8614$

$\rightarrow I_D = k_n (V_{ss}-1)^2 = 169\,\mu A$

Q19)

Q20) ~~$\frac{1}{2}$~~ $5\cdot(1) \rightarrow$ end of first : 1010

end of second $\rightarrow$

Q21) $\frac{10.7}{I_{CP}} \cdot C > T_2 - T_1$

$\frac{10.7}{I_{CP}} C > 1.5\,ms$

$I_{CP} =$

$I_{CP} = 10.7 \rightarrow 0.23 \times 10^{-4}$

$25818 \cdot C > 1.5\,ms$

$C >$

Q23) M_n linear $\rightarrow$

$I_D =$

Q24) $V_{o\,max} = \frac{I_{CP}\cdot t_s}{C}$, $t_s = 10.7 \cdot \frac{C}{I_{CP}}$

$I_{CP} = 0.4104\,44\,mA \rightarrow t_s =$ ~~1.80725~~ 1.291023

$\rightarrow V_{o\,max} =$

$C = 0.5$

Q24) M_p sat $\rightarrow I_C = k_p (V_{SG_p} - V_{TP})^2 =$